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ASNT1012 (ASNT1032)
16:1 MUX-CMU

- 16 to 1 multiplexer (MUX) with integrated CMU (clock multiplication unit).
- Supports multiple data rates in the 9.8-12.5*Gb/s* range.
- LVDS compliant input data buffers.
- Clock-divided-by-16 LVDS output buffer.
- Single +3.3*V* power supply.
- Industrial temperature range.
- Low power consumption of 660*mW* at 12.5*Gbps*.
- Available in standard 100-pin QFN package (12*mm* x 12*mm*).

DESCRIPTION

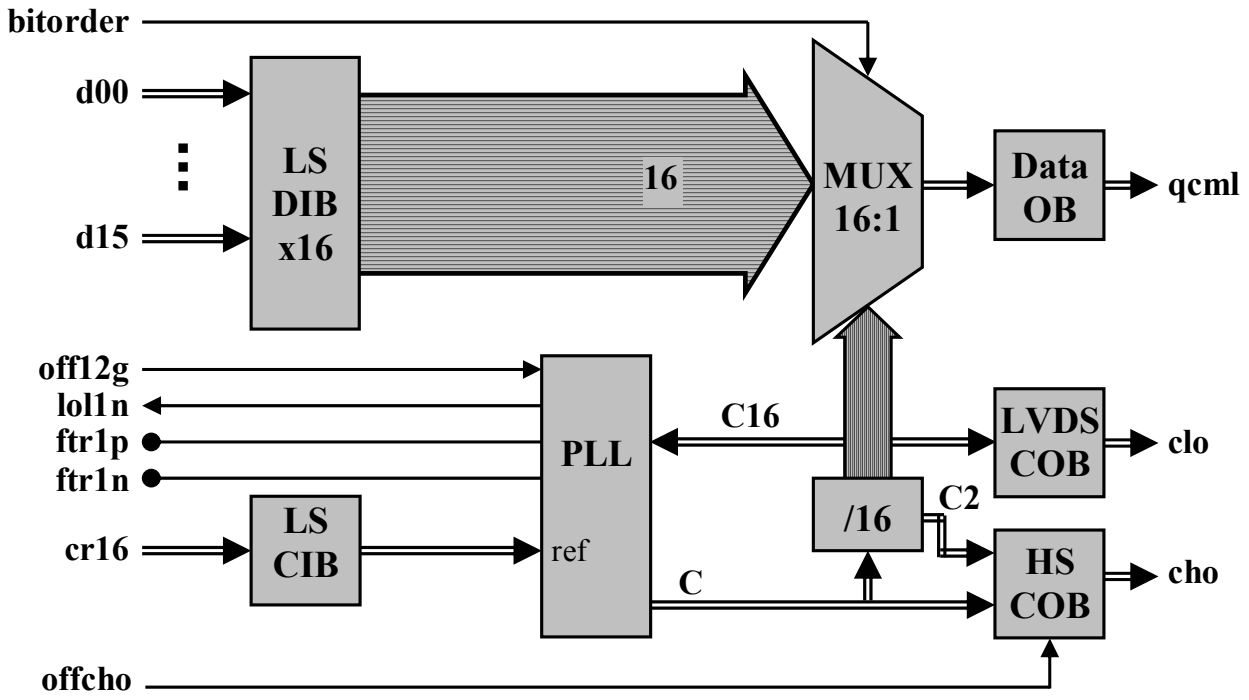

Fig. 1. Functional Block Diagram.

ASNT1012 is a low power and high-speed 16 to 1 multiplexer (MUX) with an internal clock multiplier unit (CMU). The MUX can function at data rates (f_{bit}) between 9.8*Gbps* to 12.5*Gbps* by utilizing its multiple on-chip full-rate VCOs.

The main function of ASNT1012 is to multiplex 16 parallel data channels running at a bit rate of $f_{bit}/16$ into a high speed serial bit stream running at f_{bit}. It provides a high-speed output data channel for point-to-point data transmission over a controlled impedance media of 50*Ohm*. The transmission media can be a printed circuit board or copper coaxial cables. The functional distance of the data transfer is dependent upon the attenuation characteristics of the transportation media and the degree of noise coupling to the signaling environment.

During normal operation, the serializer's low-speed input buffer (LS DIBx16) accepts external 16-bit wide parallel data words "d00"-"d15" through 16 differential LVDS inputs and delivers them to the multiplexer's core (MUX16:1) for serialization. By utilizing pin "bitorder", the serializer can designate either "d00" or "d15" as the MSB thus simplifying the interface between ASNT1012 and a proceeding ASIC.

MUX16:1 serializes the data words with multiple divided down clock signals that are generated from the full rate clock "C" by the internal divider (/16). The divider also produces half rate clock "C2" for the high speed clock output buffer (HS COB), and engenders a full rate clock divided-by-16 signal "C16" for use by the PLL (PLL). "C" is synthesized by PLL, which locks "C16" to the external system level clock "cr16" that is provided by the low speed clock input buffer (LS CIB). "cr16" must be 1/16 the frequency of the active full rate VCO in PLL. PLL contains 2 full rate VCOs to cover the 9.8-12.5*GHz* range, which are selected utilizing the "off12g" control pin.

The serialized words are transmitted as 2-level signals "qcml" by a differential CML output buffer (Data OB). A full-rate or half-rate clock "cho" is transmitted by a similar CML buffer (HS COB) in parallel with the high-speed data. The clock and data outputs are well phase matched to each other resulting in very little relative skew over the operating temperature range of the device. HS COB may be disabled or its operational mode changed by means of the 3-state (vee, vcc, not connected (n/c)) CMOS "offcho" signal. Both output stages are back terminated with on-chip 50*Ohm* resistors.

ASNT1012 also provides a differential low speed output clock "clo" though a LVDS clock output buffer (LVDS COB). PLL generates a loss of lock signal alarm "lol1n". An off chip capacitor is required for PLL and is connected through pins "ftr1p/n".

The serializer uses a single +3.3*V* power supply and is characterized for operation from −25°*C* to 125°*C* of junction temperature.

LS DIBx16

The Low-Speed Data Input Buffer (LS DIBx16) consists of 16 proprietary universal input buffers (UIBs) that exceed the LVDS standards IEEE Std. 1596.3-1996 and ANSI/TIA/EIA-644-1995. UIB is designed to accept differential signals with amplitudes above 60*mV* peak-to-peak (p-p), DC common mode voltage variation between the negative (vee) and positive (vcc) supply rails, and AC common mode noise with a frequency up to 5*MHz* and voltage levels ranging from 0 to 2.4*V*. It can also receive single-ended signals with amplitudes above 60*mV* p-p and threshold voltages between vee and vcc. The input termination impedance is set to 100*Ohm* differential.

LS CIB

The Low-Speed Clock Input Buffer (LS CIB) is a UIB that can run at a frequency up to 800*MHz*. This block is used to deliver the low speed system clock "cr16" as a reference signal to PLL.

PLL

The Phase Locked Loop (PLL) contains a phase frequency detector, charge pump, an on-chip integrator with an additional off-chip filter connected between the pins "ftr1p" and "ftr1n" (Fig. 2), and two selectable LC-tank VCOs centered at 11.8*GHz* and 11.0*GHz*. The main function of

PLL is to synthesize full rate clock "C" by aligning the phase and frequency of "C16" of the activated VCO to the externally applied system clock "cr16". A logic "0" output CMOS loss-of-lock "lol1n" alarm signal is generated by PLL if its two input clock signals are not matching in phase and/or frequency.

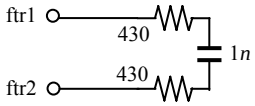

Fig. 2. External Filter Schematic.

Selection of the different VCOs of PLL is achieved by utilizing the CMOS control pin "off12g". A logic "1" chooses the 11.0*GHz* VCO while a logic "0" selects the 11.8*GHz* VCO (default state). The unused VCO is turned completely off in order to save power.

/16

The Divider-by-16 (/16) includes 4 divide-by-2 circuits connected in series. High-speed clock "C" is fed into the first divide-by-2 circuit that generates "C2". "C2" is routed internally to the next divide-by-two circuit and outside of the block to MUX16:1 and HS COB. Other divided down clock signals are formed and routed to MUX16:1 in similar fashion. "C16" is passed on to PLL and LVDS COB to become the output low speed clock signal "clo".

MUX16:1

The 16 to 1 Multiplexer (MUX16:1) utilizes a tree type architecture that latches the incoming data on the negative edge of the "C16" clock signal that is supplied by /16. The 16-bit wide data word is subsequently multiplexed and delivered to Data OB as a serial data stream running at a data rate up to 12.5*Gbps*. The latency of this circuit block is equal to roughly one period of the low-speed input clock. When "bitorder"=0 (default), "d00"is the MSB and when "bitorder"=1, "d15" is designated the MSB.

Data OB

The Data Output Buffer (Data OB) receives high-speed serial data from MUX16:1 and converts it into the CML output signal "qcml" with a single ended swing of 600*mV*. The buffer requires 50*Ohm* external termination resistors connected between "vcc" and each output to match its internal 50*Ohm* resistors and can operate at a data rate up to 12.5G*bps*.

HS COB

The High Speed Clock Output Buffer (HS COB) utilizes the same termination scheme as Data OB and can operate at a frequency up to 12.5*GHz* while producing a single-ended CML output swing of 600*mV*. The buffer can be enabled or disabled by the external 3-state (vcc, vee, not connected (n/c)) control signal "offcho". The n/c default state corresponds to a "C2" output signal. The logic "0" state provides a full-rate clock output signal while the logic "1" state disables the buffer completely to save power.

LVDS COB

The LVDS Clock Output Buffer (LVDS COB) receives "C16" from /16 and converts it into a LVDS output signal "clo". The proprietary low-power LVDS output buffer utilizes a special architecture that ensures operation at frequencies up to 2*GHz* with a low power consumption level of 30*mW*. The buffer satisfies all the requirements of the IEEE Std. 1596.3-1996 and ANSI/TIA/EIA-644-1995.

Output Timing

Phase relation between the output data "qcml" and full rate output clock "cho" is specified in Table 1 and illustrated by Fig. 3.

Table 1. Output Data-to-Clock Phase Difference

Junction temperature, ^oC	τ, *ps*	
	Min.	Max.
-25	77	80
50	82	86
125	87	91

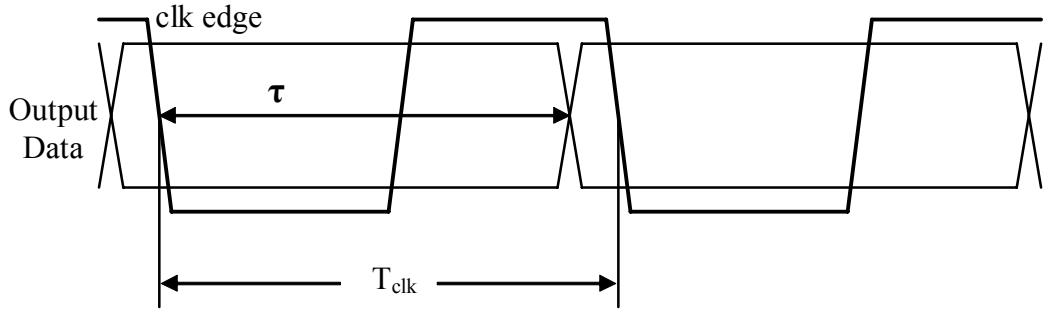

Fig. 3. Output Timing Diagram

TERMINAL FUNCTIONS

The description of the package pins is presented in the table below.

TERMINAL			DESCRIPTION
Name	No.	Type	
High-Speed I/Os			
chop	37	Output	CML differential clock outputs. Require external SE 50*Ohm* termination to "vcc". Can be disabled by "offcho".
chon	36		
qcmlp	43	Output	CML differential data outputs. Require external SE 50*Ohm* termination to "vcc".
qcmln	42		
Controls			
lol1n	21	LS Out, CMOS	PLL lock indicator (high: locked; low: no lock).
ftr1p	22	I/O	PLL external filter connection (1*nF* capacitor differential).
ftr1n	23		
offcho	20	LS In., 3-state	HS COB control (active: high, buffer is disabled; active: low, full-rate clock; default: not connected, half-rate clock).
off12g	24	LS In., CMOS	VCO frequency selection (active: high, 11.0*GHz*; default: low, 11.8*GHz*).
bitorder	60	LS In., CMOS	Input bit order selection (active: high, d15 is serialized first; default: low, d00 is serialized first).

Low-Speed I/Os			
cr16p	14	Input	LVDS clock inputs.
cr16n	15		
clop	48	Output	LVDS clock outputs.
clon	47		
d00p	61	Input	LVDS data inputs.
d00n	62		
d01p	64		
d01n	65		
d02p	67		
d02n	68		
d03p	70		
d03n	71		
d04p	76		
d04n	77		
d05p	79		
d05n	80		
d06p	82		
d06n	83		
d07p	85		
d07n	86		
d08p	88		
d08n	89		
d09p	90		
d09n	91		
d10p	93		
d10n	94		
d11p	96		
d11n	97		
d12p	99		
d12n	100		
d13p	5		
d13n	6		
d14p	8		
d14n	9		
d15p	11		
d15n	12		

Supply and Termination Voltages		
Name	**Description**	**Pin Number**
vcc	Positive power supply. (+3.3*V*)	1, 7, 10, 13, 16, 29, 32-35, 38-41, 44, 45, 49, 55, 63, 66, 69, 72, 78, 81, 84, 87, 92, 95, 98.
vee	Negative power supply. (GND or 0*V*)	3, 17, 25, 26, 50, 51, 58.
nc	Unconnected pin.	2, 18, 19, 27, 28, 30, 31, 46, 53-54, 56, 57, 59, 73-75.

ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
V_{CC}	+3.14	+3.3	+3.47	*V*	±5%
V_{EE}		0.0		*V*	
Power consumption		660		*mW*	
Junction temperature	-25	50	125	*°C*	
LS Input Data (d00-d15)					
Data Rate	612.5		780	*Mbps*	
Differential Swing	0.06		0.8	*V*	Peak-to-peak
CM Voltage Level	V_{EE}		V_{CC}	*V*	
LS Input Reference Clock (cr16)					
Frequency	612.5		780	*MHz*	
Differential Swing	0.06		0.8	*V*	Peak-to-peak
CM Voltage Level	V_{EE}		V_{CC}	*V*	
HS Output Data (qcml)					
Data Rate	9.8		12.5	*Gbps*	
Logic “1” level		V_{CC}		*V*	
Logic “0” level		V_{CC}-0.6		*V*	
Jitter		12		*ps*	Peak-to-peak @12.5*Gb/s*
HS Output Clock (cho)					
Frequency	4.9		12.5	*GHz*	
Logic “1” level		V_{CC}		*V*	
Logic “0” level		V_{CC}-0.6		*V*	
Jitter		6		*ps*	Peak-to-peak @12.5*GHz*
Duty Cycle		50%			
LS Output Clock (clo)					
Frequency	612.5		780	*MHz*	
Interface		LVDS			Meets the IEEE Std.
CMOS Control Inputs/Outputs					
Logic “1” level	V_{CC}-0.4			*V*	
Logic “0” level			V_{EE}+0.4	*V*	

PACKAGE INFORMATION

The chip is packaged in a standard 100-pin QFN package. The package’s mechanical information is available on the company’s website.