27 Via Porto Grande, Rancho Palos Verdes, CA, 90275. Ph. # 1-310-377-6029. Fax # 1-310-377-9940.

ASNT2012 (2032)
1:16 CDR-DMUX

- 1:16 demultiplexer (DMUX) with integrated full rate CDR (clock and data recovery).
- Supports multiple data rates in the 11.3-12.5*Gbps* range.
- Supports NRZ input data format.
- LVDS output data buffers that feature a low-power proprietary architecture.
- Clock-divided-by-16 LVDS output buffer with 90°-step phase selection.
- Single +3.3*V* power supply.
- Industrial temperature range.
- Low power consumption of 730*mW* at 12.5*Gbps*.
- Available in standard 100-pin QFN package (12*mm* x 12*mm*).

DESCRIPTION

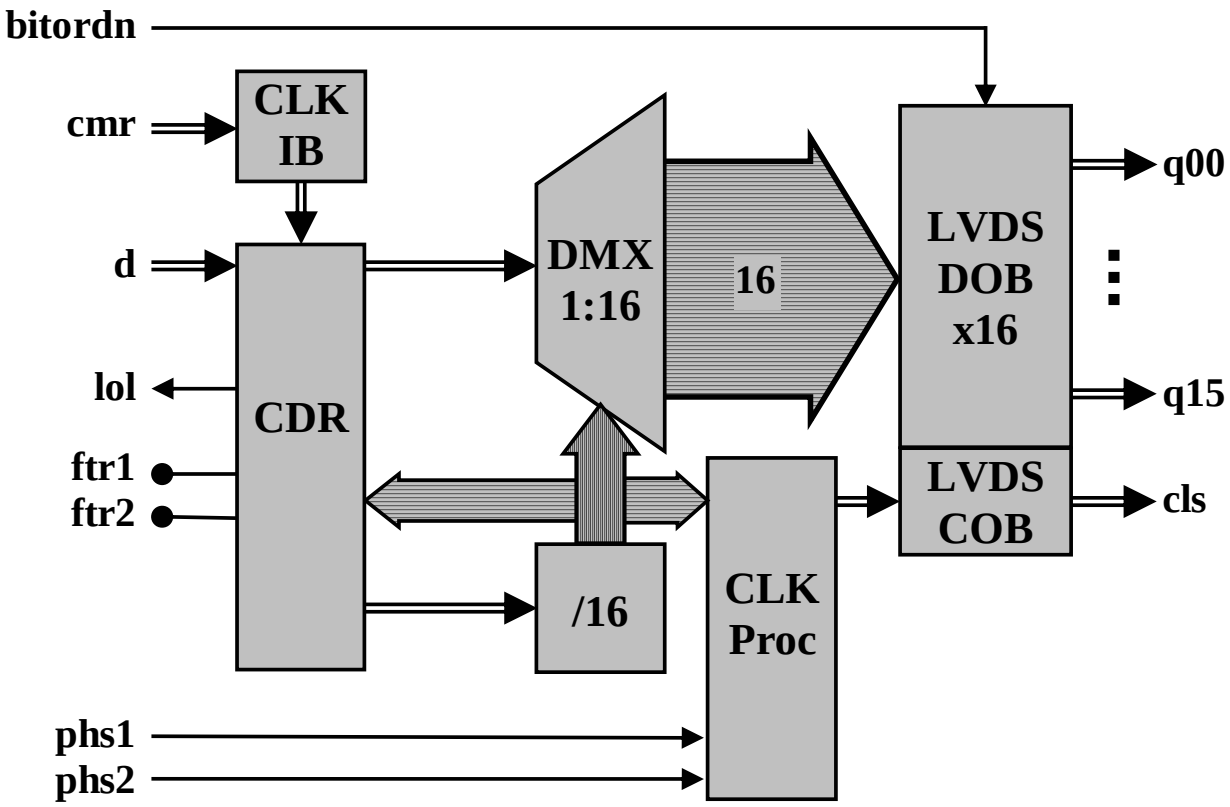

Fig. 1. Functional Block Diagram.

ASNT2012 is a 12.5*Gbps* 1:16 deserializer (DMUX) with full rate integrated clock and data recovery (CDR). The DMUX can cover input data rates (f_{bit}) from 11.3*Gbps* to 12.5*Gbps* by utilizing its on-chip full-rate VCO.

The main function of ASNT2012 is to demultiplex a serial input data channel "d" running at a bit rate of f_{bit} into 16 parallel data channels "q00-q15" running at a bit rate of $f_{bit}/16$. The high sensitivity CDR block ensures accurate clock and data recovery for input data signal amplitudes greater than 40*mV* peak to peak (p-p) differential or single-ended. This is accomplished with the CDR circuitry incorporating both a phase and frequency acquisition loop to recover a full rate clock "C" from the input data stream. This recovered clock is used to sample the input data bits before they are demultiplexed and provides a signal for the internal divider (/16). The application of an external low speed system clock "cmr" running at 1/16 the frequency of the VCO clock is required for CDR to operate correctly.

The high-speed CML data input buffer in CDR provides on-chip 50*Ohm* termination and is designed to be driven by devices with 50*Ohm* source impedance. The low speed clock input buffer (CLK IB) accepts the system reference clock "cmr" through a LVDS interface and delivers it to the CDR block.

The reconstructed serial input data is latched into the tree-type demultiplexer (DMX1:16) and subsequently deserialized and delivered to the demultiplexer's output as 16-bit wide low-speed parallel words. Utilizing pin "bitordn", the deserializer can designate either "q00" or "q15" as the MSB thus simplifying the interface between ASNT2012 and a following ASIC.

Sixteen proprietary low-power LVDS output data buffers (LVDS DOBx16) are used to deliver the 16 data output signals "q00-q15" while a similar LVDS clock output buffer (LVDS COB) outputs the low-speed clock signal "cls". The buffers satisfy all the requirements of the IEEE Std. 1596.3-1996 and ANSI/TIA/EIA-644-1995 while only consuming 30*mW* each. The phase of "cls" can be modified by 90° increments by utilizing pins "phs1" and "phs2" and the low speed clock processing block (CLK Proc).

A loss of lock system signal alarm "lol" is generated by CDR. Off chip passive filter components are required by CDR and are connected through pins "ftr1/2".

The deserializer uses a single +3.3*V* power supply and is characterized for operation from −25°*C* to 125°*C* of junction temperature.

CDR

The Clock and Data Recovery Block (CDR) contains both a phase and frequency acquisition loop that require an additional off-chip filter connected between the pins "ftr1p" and "ftr1n" (***Fig. 2***). The frequency loop works in concert with "cmr" while the phase loop utilizes "d".

Fig. 2. External Filter Schematic.

The main function of CDR is to frequency lock the on-chip VCO to the input data signal (clock recovery) while phase aligning it to latch in the incoming data with minimal error (data recovery). The recovered clock is also utilized by /16 and DMX 1:16 to demultiplex the data.

The lock detect circuitry signals an alarm through the CMOS signal "lol" when a frequency difference exists between the applied system reference clock "cmr" and recovered full rate clock divided-by-16 that is greater than ±1000*ppm*.

CLK IB

The Clock Input Buffer (CLK IB) consists of a proprietary universal input buffer (UIB) that exceeds the LVDS standards IEEE Std. 1596.3-1996 and ANSI/TIA/EIA-644-1995. UIB is designed to accept differential signals with amplitudes higher than 60*mV* p-p, DC common mode voltage variation between the negative (vee) and positive (vcc) supply rails, and AC common mode noise with a frequency up to 5*MHz* and voltage levels ranging from 0 to 2.4*V*. It can also receive single-ended signals with amplitudes of more than 60*mV* p-p and threshold voltages between vee and vcc. The input termination impedance is set to 100*Ohm* differential.

/16

The Divider-by-16 (/16) includes 4 divide-by-2 circuits connected in series. The high-speed clock "C" delivered by CDR is fed into the first divide-by-2 where its output is routed internally to the next divide-by-two circuit and outside of the block to DMX1:16. Other divided down clock signals are formed and routed to DMX1:16 in similar fashion. Full rate clock divided-by-16 "C16" is passed on to CLK Proc for additional phase adjustment.

DMX1:16

The 1 to 16 Demultiplexer (DMX1:16) utilizes a tree type architecture that latches in the data stream from CDR on both edges of a half rate clock signal that is supplied by /16. The high speed data signal is subsequently demultiplexed down and delivered to LVDS DOBx16 in parallel fashion as16-bit wide words running at a data rate up to 780*Mbps*.

CLK Proc

By utilizing the CMOS control pins "phs1" and "phs2", the phase of "cls" can be altered in accordance with the table below.

"phs1"	"phs2"	C16S phase
V_{EE} (default)	V_{EE} (default)	270°
V_{EE}	V_{CC}	180°
V_{CC}	V_{EE}	90°
V_{CC}	V_{CC}	0°

LVDS DOBx16

The LVDS Data Output Buffer (LVDS DOBx16) accepts 16-bit wide words from DMX1:16 and converts them into LVDS output signals. Each proprietary low-power LVDS output buffer utilizes a special architecture that ensures operation at bit rates up to 2*Gb/s* with a low power

consumption level of 30*mW*. The buffer satisfies all the requirements of the IEEE Std. 1596.3-1996 and ANSI/TIA/EIA-644-1995. When "bitorder"=0 (default), "q00"is the MSB and when "bitorder"=1, "q15" is designated the MSB.

LVDS COB

The LVDS Clock Output Buffer (LVDS COB) receives "C16" from CLK Proc and converts it into the LVDS output signal "cls". The proprietary low-power LVDS output buffer utilizes a special architecture that ensures operation at frequencies up to 2*GHz* with a low power consumption level of 30*mW*. The buffer satisfies all the requirements of the IEEE Std. 1596.3-1996 and ANSI/TIA/EIA-644-1995.

Terminal Functions

The description of the package pins is presented in the table below.

TERMINAL			DESCRIPTION
Name	No.	Type	
Low-Speed I/Os			
cmrp	31	Input	LVDS reference clock inputs for CDR.
cmrn	30		
q00n	12	Output	LVDS data outputs.
q00p	11		
q01n	9		
q01p	8		
q02n	6		
q02p	5		
q03n	100		
q03p	99		
q04n	97		
q04p	96		
q05n	94		
q05p	93		
q06n	91		
q06p	90		
q07n	89		
q07p	88		
q08n	86		
q08p	85		
q09n	83		
q09p	82		
q10n	80		

q10p	79		
q11n	77		
q11p	76		
q12n	71		
q12p	70		
q13n	68		
q13p	67		
q14n	65		
q14p	64		
q15n	62		
q15p	61		
clsp	14	Output	LVDS clock outputs. Can transmit four different clock phases as defined by "phs1" and "phs2".
clsn	15		
High-Speed I/Os			
dp	43	Input	CML differential data inputs with internal SE 50*Ohm* termination to "vcc".
dn	42		
Controls			
phs1	57	LS In., CMOS	Low-speed output clock phase selection (default: both low).
phs2	56		
lol	21	LS Out, CMOS	CDR lock indicator (high: locked; low: no lock).
ftr1	22	I/O	External CDR filter connections.
ftr2	23		
bitordn	18	LS In., CMOS	Output bit order selection (active: high, q15 is MSB; default: low, q00 is MSB).

Supply and Termination Voltages

Name	Description	Pin Number
vcc	Positive power supply. (+3.3*V*)	1, 7, 10, 13, 16, 19, 29, 32-35, 38-41, 44, 45, 52, 55, 60, 63, 66, 69, 72, 78, 81, 84, 87, 92, 95, 98.
vee	Negative power supply. (GND or 0*V*)	3, 17, 25, 49-51, 58.
nc	Unconnected pin.	2, 4, 20, 24, 26-28, 36, 37, 46-48, 53, 54, 59, 73-75.

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ELECTRICAL CHARCTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
		General Parameters			
V_{CC}	+3.14	+3.3	+3.47	*V*	±5%
V_{EE}		0.0		*V*	
Power consumption		730		*mW*	
Junction temperature	-25	50	125	*°C*	
		HS Input Data (d)			
Data Rate	11.3		12.5	*Gbps*	
Swing (Diff or SE)	0.04		1.2	*V*	Peak-to-peak
CM Voltage Level	V_{CC}-0.8		V_{CC}	*V*	
		LS Input Reference Clock (cmr)			
Frequency	700		780	*MHz*	
Swing (Diff or SE)	0.06		0.8	*V*	Peak-to-peak
CM Voltage Level	V_{EE}		V_{CC}	*V*	
Duty Cycle	40%	50%	60%		
		LS Output Data (q00-q15)			
Data Rate	700		780	*Mbps*	
Interface		LVDS			Meets the IEEE Std. 1596.3-1996
		LS Output Clock (cls)			
Frequency	700		780	*MHz*	
Interface		LVDS			Meets the IEEE Std. 1596.3-1996
		CMOS Control Inputs/Outputs			
Logic “1” level	V_{CC}-0.4			*V*	
Logic “0” level			V_{EE}+0.4	*V*	
		Timing Parameters			
“cls” to “q0-q15” delay variation		±2.5%			Over the full temperature range

PACKAGE INFORMATION

The chip is packaged in a standard 100-pin QFN package. The package’s mechanical information is available on the company’s website.