ADSANTEC
Ultra High-Speed Mixed Signal ASICs

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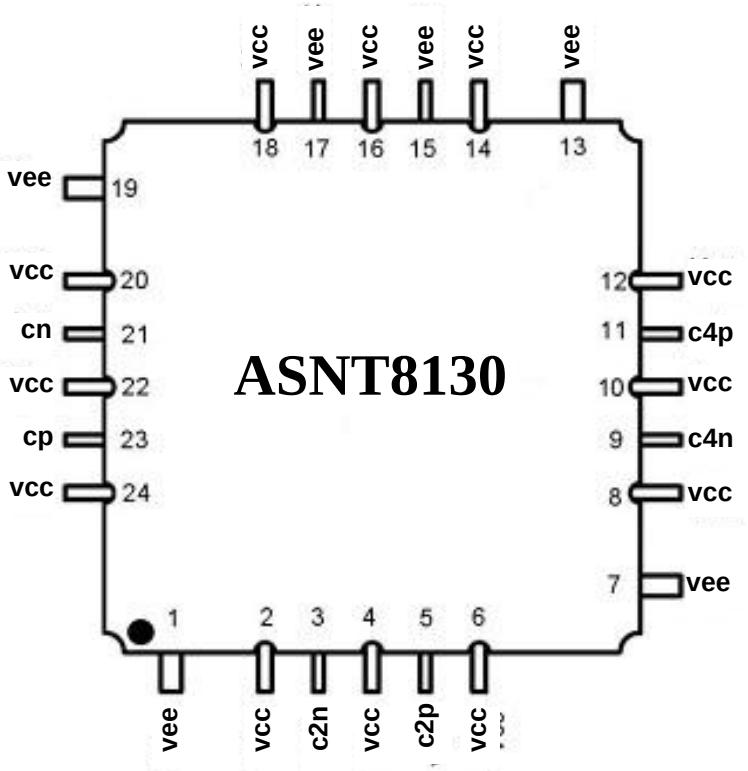
# ASNT8130-KMC

# 36*GHz* Divider by 2 and by 4

- Wide frequency range from DC to 36*GHz*
- Divided-by-2 and divided-by-4 outputs
- 50% duty cycle of the divided clock signal
- Fully differential CML input interface
- Fully differential CML output interface
- Single +3.3*V* or -3.3*V* power supply
- Industrial temperature range
- Power consumption of 260*mW* at full operational speed
- Custom CQFP 24-pin package



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# DESCRIPTION

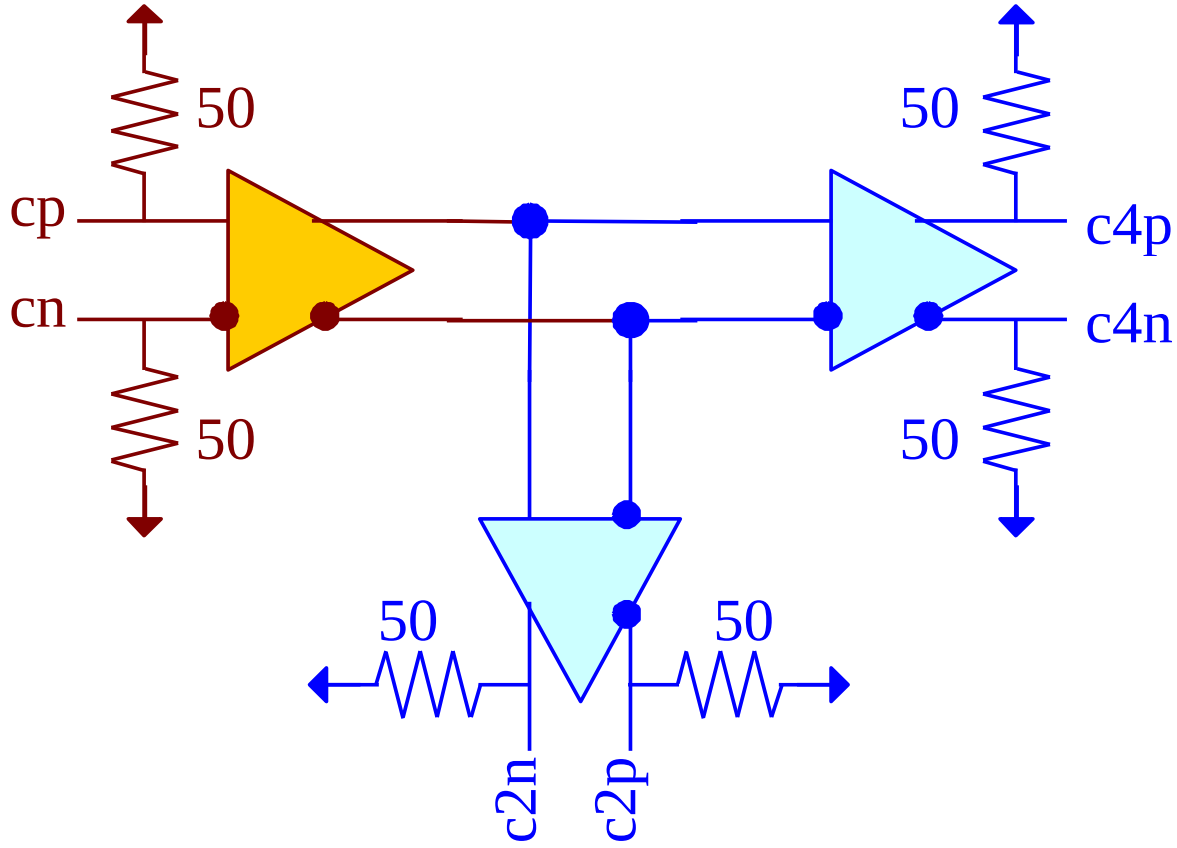


*Fig. 1. Functional Block Diagram*

ASNT8130-KMC is a high-speed, low-power divider by-2 and by-4. The part shown in Fig. 1 accepts a CML input clock signal (cp/cn) with the speed from DC to maximum operational frequency and provides clean 50% duty cycle output signals with divided-by-2 (c2p/c2n) and divided-by-4 (c4p/c4n) frequency.

The part's I/Os support the CML logic interface with on chip 50*Ohm* termination to vcc and may be used differentially, AC/DC coupled, single-ended, or in any combination (see also POWER SUPPLY CONFIGURATION). In the DC-coupling mode, the input signal's common mode voltage should comply with the specifications shown in ELECTRICAL CHARACTERISTICS. In the AC-coupling mode, the input termination provides the required common mode voltage automatically. The differential DC signaling mode is recommended for optimal performance.

# POWER SUPPLY CONFIGURATION

The ASNT8130-KMC can operate with either negative supply (vcc = 0.0*V* =ground and vee = -3.3*V*), or positive supply (vcc = +3.3*V* and vee = 0.0*V* = ground). In case of the positive supply, all I/Os need AC termination when connected to any devices with 50*Ohm* termination to ground. Different PCB layouts will be needed for each different power supply combination.

**All the characteristics detailed below assume vcc = 0.0*V* and vee = -3.3*V*.**

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# ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in *Table 1* may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground (assumed vcc).

*Table 1. Absolute Maximum Ratings*

| Parameter | Min | Max | Units |
|---|---|---|---|
| Supply Voltage (vee) | | -3.6 | *V* |
| Power Consumption | | 0.29 | *W* |
| RF Input Voltage Swing (SE) | | 1.0 | *V* |
| Case Temperature | | +90 | *°C* |
| Storage Temperature | -40 | +100 | *°C* |
| Operational Humidity | 10 | 98 | *%* |
| Storage Humidity | 10 | 98 | *%* |

# TERMINAL FUNCTIONS

| TERMINAL | | | DESCRIPTION |
|---|---|---|---|
| **Name** | **No.** | **Type** | |
| **High-Speed I/Os** | | | |
| cp | 23 | CML input | Differential clock input with internal SE 50*Ohm* termination to vcc |
| cn | 21 | | |
| c2p | 5 | CML output | Differential divided clock outputs with internal SE 50*Ohm* termination to vcc. Require external SE 50*Ohm* termination to vcc |
| c2n | 3 | | |
| c4p | 11 | | |
| c4n | 9 | | |

| Supply and Termination Voltages | | |
|---|---|---|
| Name | Description | Pin Number |
| vcc | Positive power supply (+3.3*V* or 0*V*) | 2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24 |
| vee | Negative power supply (0*V* or -3.3*V*) | 1, 7, 13, 15, 17, 19 |

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# ELECTRICAL CHARACTERISTICS

| PARAMETER | MIN | TYP | MAX | UNIT | COMMENTS |
|---|---|---|---|---|---|
| **General Parameters** | | | | | |
| vee | -3.1 | -3.3 | -3.5 | *V* | ±6% |
| vcc | | 0.0 | | *V* | External ground |
| *I*vee | | 79 | | *mA* | |
| Power consumption | | 260 | | *mW* | |
| Junction temperature | -25 | 50 | 125 | *°C* | |
| **HS Input Clock (cp/cn)** | | | | | |
| Frequency | 0 | | 36 | *GHz* | |
| Swing | 60 | | 800 | *mV* | Differential or SE, p-p |
| CM Voltage Level | vcc-0.8 | vcc-0.2 | vcc | *mV* | Must match for both inputs |
| **Output Divided Clock (c2p/c2n, c4p/c4n)** | | | | | |
| Frequency *f*/2 | 0 | | 18 | *GHz* | For c2 out signal |
| Frequency *f*/4 | 0 | | 9 | *GHz* | For c4 out signal |
| Logic "1" level | | vcc | | *V* | |
| Logic "0" level | | vcc-0.35 | | *V* | With external 50*Ohm* DC termination |
| Duty cycle | 45 | 50 | 55 | *%* | |
| Additive Jitter | | TBD | | *ps* | Peak-to-peak |

# PACKAGE INFORMATION

The chip die is housed in a custom 24-pin CQFP package shown in Fig. 2. The package provides a center heat slug located on its back side to be used for heat dissipation. ADSANTEC recommends for this section to be soldered to the vcc plain, which is ground for a negative supply, or power for a positive supply.

The part's identification label is ASNT8130-KMC. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package's manufacturer, type, and pin out count.

This device complies with the Restriction of Hazardous Substances (RoHS) per 2011/65/EU for all ten substances.

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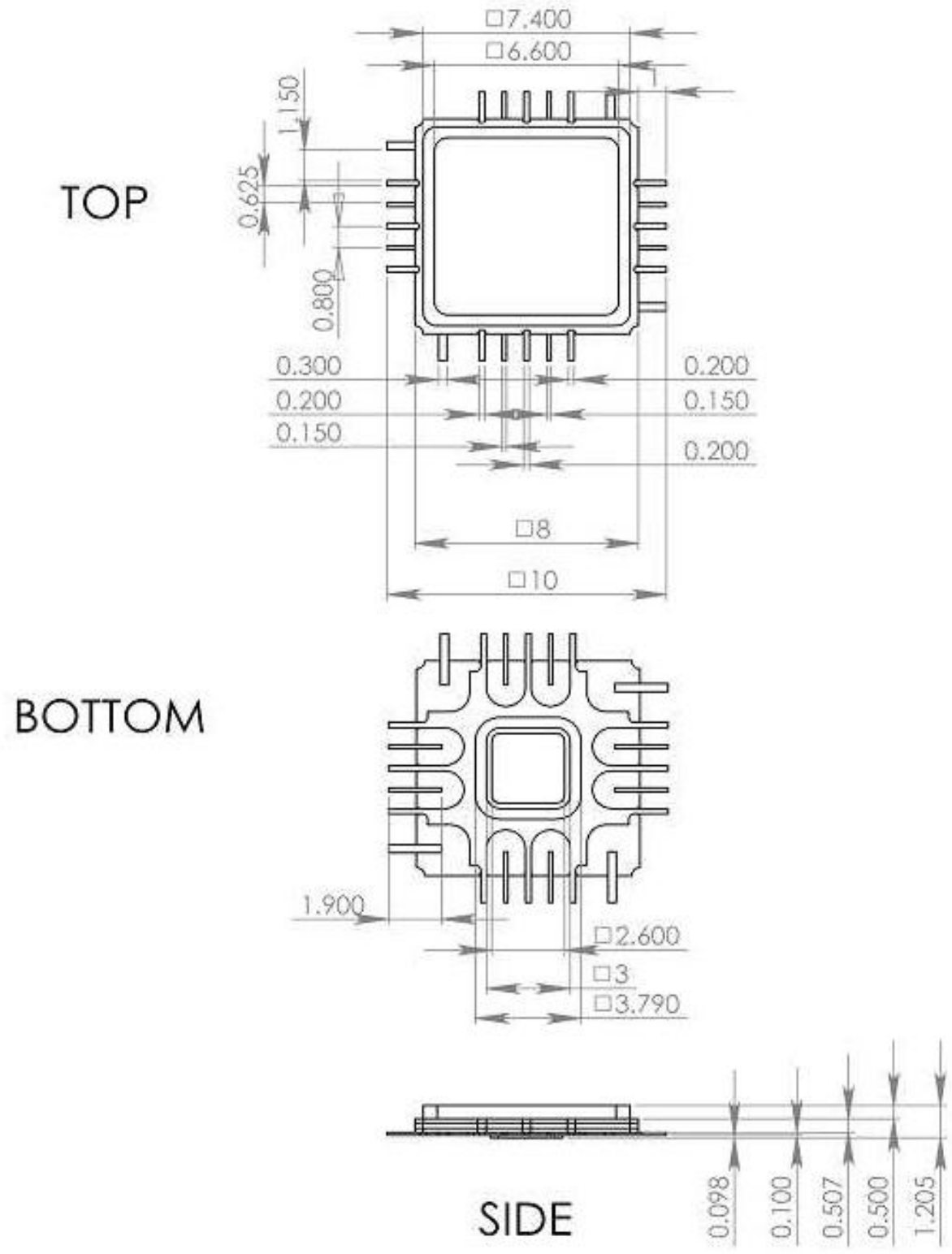


*Fig. 2. CQFP 24-Pin Package Drawing (All Dimensions in mm)*

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# REVISION HISTORY

| Revision | Date | Changes |
|---|---|---|
| 2.5.2 | 02-2020 | Updated Package Information |
| 2.4.2 | 07-2019 | Updated Letterhead |
| 2.4.1 | 12-2016 | Corrected description<br>Corrected specification of the output swing |
| 2.3.1 | 08-2014 | Corrected operating frequency range |
| 2.2.1 | 01-2013 | Correction: output Diff Swing instead of SE<br>Format correction |
| 2.1.1 | 01-2013 | Added package drawing<br>Corrected Absolute Maximum Ratings<br>Corrected current and power consumption<br>Corrected format |
| 2.0.1 | 06-2012 | Added pin out drawing<br>Added Power Supply Configuration text<br>Added Absolute Maximum Ratings table<br>Revised Electrical Characteristics section<br>Added Package Information section<br>Added Revision History |
| 1.0 | 09-2011 | First release |