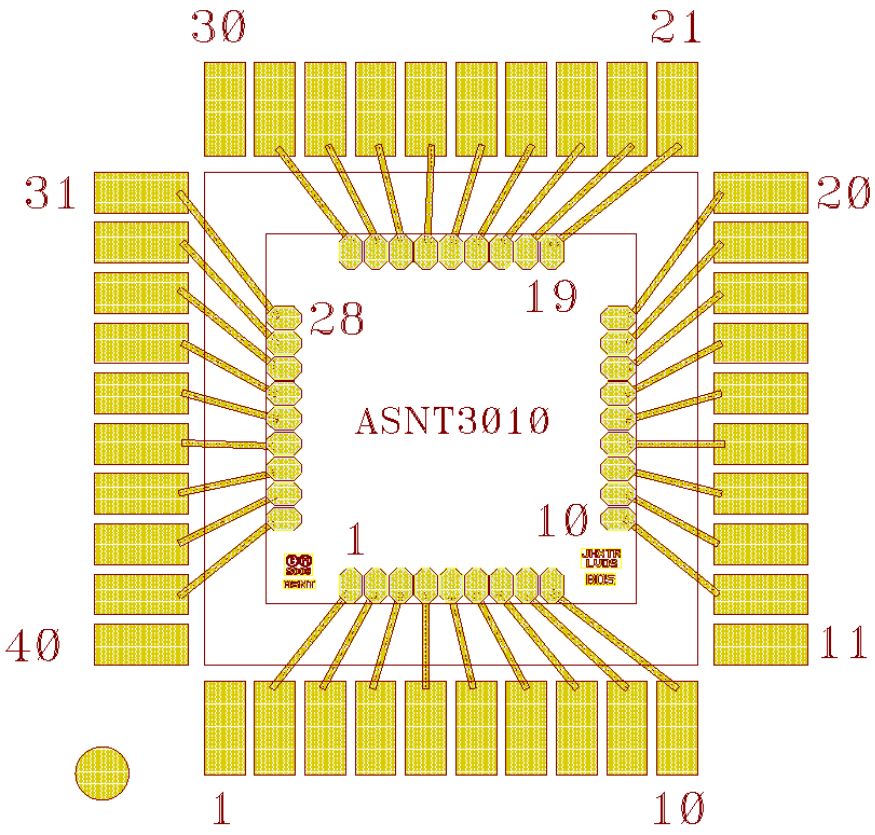
ADSANTEC
Advanced Science and Novel Technology
27 Via Porto Grande, Rancho Palos Verdes, CA, 90275. Ph. # 1-310-377-6029. Fax # 1-310-377-9940.

# ASNT3010_QQB
# 2*Gbps* LVDS/CMOS/LVDS Converter and Signal Splitter

- 2-channel LVDS-to-CMOS converter (Receiver).
- 2-channel CMOS-to-LVDS converter (Transmitter).
- Triple-action programmable LVDS/CML/ECL inputs.
- Optional DS (Data/Strobe) encoding/decoding for compatibility with Space Wire Standard.
- Optional signal splitter function with selectable inversion.
- Flexible selection of channels enabling and operational modes.
- High-impedance states of disabled CMOS outputs.
- Single +3.3*V* power supply.
- Industrial temperature range.
- Power consumption: 115*mW* with all 4 channels enabled.
- Package: 40-pin MLF with 6x6$mm^2$ body size and 0.5*mm* lead pitch.

## *ASNT3010 BONDING DIAGRAM*



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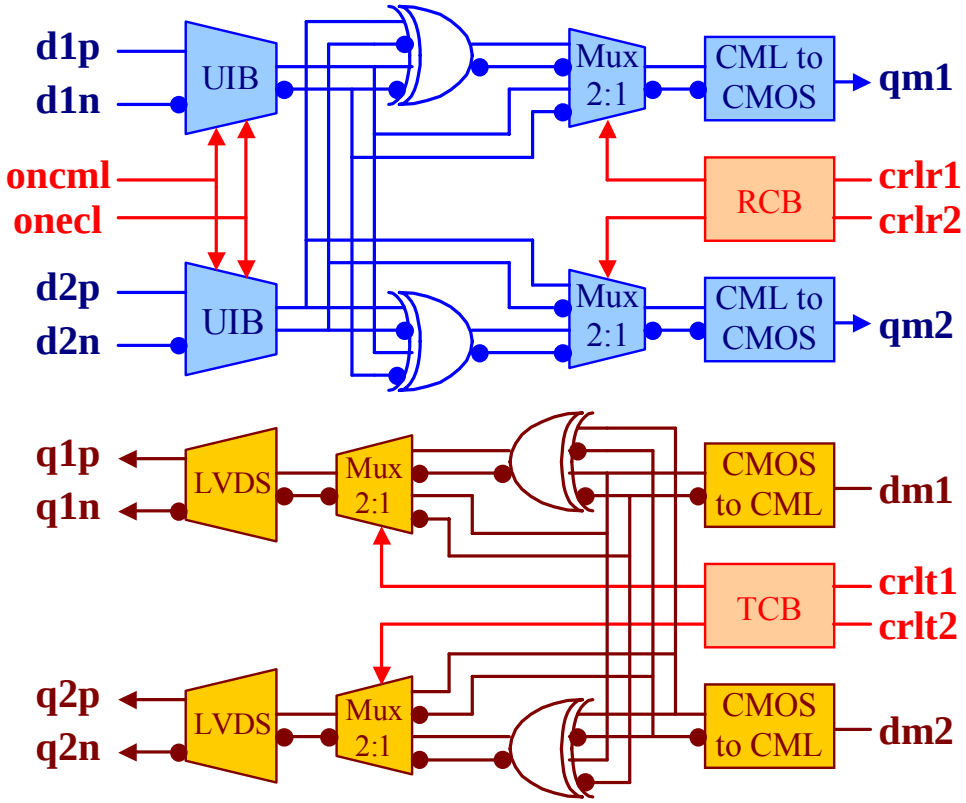
## *DESCRIPTION*




ASNT3010 is a bi-directional 4-channel digital interface converter. It includes two independent "Receiver" channels with programmable LVDS/CML/ECL differential inputs ("d1p/n", "d2p/n") and CMOS outputs ("qm1', "qm2"), as well as two reverse "Transmitter" channels with CMOS inputs ("dm1", "dm2") and LVDS differential outputs ("q1p/n", "q2p/n").

All channels can be independently enabled or disabled by control signals ("crlr1", "crlr2", "crlt1", "crlt2"). When disabled, the CMOS output drivers are set to a high impedance (high-Z) state. Both receiver and transmitter channel pairs can be combined into a Space Wire receiver/transmitter with optional data/strobe (DS) encoding or decoding. The assignment of data and strobe or data and clock signals to the individual channels is user-selectable.

Dual transmitter and/or receiver channels can be used for splitting one of the input signals into two exact copies at two corresponding outputs. The signal at the second output can be inverted using the second input as a selector (a differential DC signal must be applied). Detailed instructions for using this operational mode are available on request.

The converter operates at data rates up to 2*Gbps* with a nominal power consumption of 115*mW* from a single +3.3*V* power supply in a fully activated mode. The device is characterized for operation from −25°C to 125°C of junction temperature.

The converter has an improved TID tolerance due to the HBT-based implementation.

## Universal IB

The proprietary Universal Input Buffer (UIB) is designed to accept differential signals with amplitudes higher than 60*mV*, DC common mode voltage variation between the negative and positive supply voltages, and AC common mode noise with a frequency up to 5*MHz* and voltage levels ranging from 0 to 2.4*V*. It can also receive single-ended signals with amplitudes of more than 60*mV* and threshold voltages between the negative and positive supply rails. The buffer outputs standard internal CML signals with amplitude of 220*mV*.

The buffer features a reconfigurable input block with internal LVDS, CML, or ECL termination that is controlled by two external CMOS signals "oncml" and "onecl" in accordance with the following table.

| "oncml" value | "onecl" value | Termination | | |
|---|---|---|---|---|
| | | Type | Resistance | Voltage |
| $V_{CC}$ | $V_{EE}$ (default) | Single-ended (SE) | 50*Ohm* | $V_{CC}$ |
| $V_{EE}$ (default) | $V_{CC}$ | Single-ended (SE) | 50*Ohm* | $V_{ECL}$ |
| $V_{EE}$ (default) | $V_{EE}$ (default) | Differential | 100*Ohm* | - |

The ECL termination mode requires an external termination voltage of $V_{ECL}=V_{CC}-2V$ applied to the pins labeled "vecl". The buffer is set to work with incoming LVDS data by default.

## CML-to-CMOS Converter

The CML-to-CMOS converter represents the output buffer of the Receiver. It includes a signal converter based on the current mirror architecture and an output CMOS driver. The block designed in a BiCMOS configuration operates at a data rate up to 2*Gbps*.

## CMOS-to-CML Converter

The input CMOS-to-CML converter represents the input buffer of the Transmitter. It is designed as a standard CML buffer with additional resistive dividers required for the handling of rail-to-rail CMOS signals.

## LVDS Output Buffer

The proprietary LVDS output buffer utilizes NPN HBTs that are available in standard BiCMOS technologies. It accepts the internal CML signals and converts them into output LVDS signals. The buffert utilizes a special architecture that ensures operation at data rates up to 2*Gbps* with a low power consumption level of 19*mW*. The buffer satisfies all the requirements of the IEEE Std. 1596.3-1996 and ANSI/TIA/EIA-644-1995.

## Internal Data Processing Circuitry

The internal parts of all 4 channels include an XOR and multiplexer 2:1 CML cells. When activated, the XOR performs the DS encoding or decoding required by the Space Wire protocol, while the multiplexer operates as a selector between the channel's input signal or XOR-processed signals. The corresponding control signals are generated by the receiver or transmitter control blocks (RCB or TCB) from 3-state external activation control signals.

Each channel can function as an independent converter, as well as a data/strobe or clock/strobe Space Wire encoder/decoder in accordance with the following table. In the second mode, the device can also perform the 1-to-2 data splitting operation (described in Application notes).

| "crlt1"/"crlr1" | "crlt2"/"crlr2" | Channel 1 (T or R) | Channel 2 (T or R) |
|---|---|---|---|
| $V_{EE}$ | $V_{EE}$ | **off** | **off** |
| $V_{EE}$ | N/C (Default) | **off** | **on** |
| $V_{EE}$ | $V_{CC}$ | **off** | **on** |
| N/C (Default) | $V_{EE}$ | **on** | **off** |
| N/C (Default) | N/C (Default) | **on** | **on** |
| N/C (Default) | $V_{CC}$ | **Data** | **Strobe/Clock** |
| $V_{CC}$ | $V_{EE}$ | **on** | **off** |
| $V_{CC}$ | N/C (Default) | **Strobe/Clock** | **Data** |
| $V_{CC}$ | $V_{CC}$ | **on** | **on** |

## *TERMINAL FUNCTIONS*

| Name | Number | Type | DESCRIPTION |
|---|---|---|---|
| vcc | 3,8,16,22 | PS | Positive power supply |
| vee | 2,6,10,17,25,29 | PS | Negative power supply (analog ground) |
| veed | 21 | PS | Digital ground |
| vecl | 28 | PS | ECL input termination voltage |
| n/c | 1,11,30,40 | - | Floating package pin |
| rfbL | 4 | Control | Internal reference voltages. Used only in test operational modes. **For normal operation must be left not connected.** |
| rfb2_2 | 5 | Control | |
| rfb2_1 | 23 | Control | |
| rfb1_1 | 24 | Control | |
| rfp | 7 | Control | |
| crlt2 | 12 | Control | Transmitter channel 2 activation control signal |
| crlt1 | 15 | Control | Transmitter channel 1 activation control signal |
| crlr1 | 20 | Control | Receiver channel 1 activation control signal |
| oncml | 26 | Control | Activation of the input CML termination mode |
| onecl | 27 | Control | Activation of the input ECL termination mode |
| crlr2 | 35 | Control | Receiver channel 2 activation control signal |
| vcm | 9 | DC voltage | CMOS input threshold voltage, default: $(V_{CC}+V_{EE})/2$ |
| dm2 | 13 | Input | Transmitter channel 2 SE CMOS input |
| dm1 | 14 | Input | Transmitter channel 1 SE CMOS input |
| qm2 | 18 | Output | Receiver channel 2 SE CMOS output |
| qm1 | 19 | Output | Receiver channel 1 SE CMOS output |
| d1p | 31 | Input | Receiver channel 1 LVDS direct input |
| d1n | 32 | Input | Receiver channel 1 LVDS inverted input |
| d2p | 33 | Input | Receiver channel 2 LVDS direct input |
| d2n | 34 | Input | Receiver channel 2 LVDS inverted input |
| q1p | 36 | Output | Transmitter channel 1 LVDS direct output |
| q1n | 37 | Output | Transmitter channel 1 LVDS inverted output |
| q2p | 38 | Output | Transmitter channel 2 LVDS direct output |
| q2n | 39 | Output | Transmitter channel 2 LVDS inverted output |

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# *ELECTRICAL CHARACTERISTICS*

| PARAMETER | MIN | TYP | MAX | UNIT | COMMENTS |
|---|---|---|---|---|---|
| ***General Parameters*** | | | | | |
| $V_{CC}$ | 3.14 | 3.3 | 3.47 | *V* | ±5% |
| $V_{EE}$ | | 0.0 | | *V* | LVDS grownd |
| $V_{EED}$ | | 0.0 | | *V* | CMOS ground |
| $V_{ECL}$ | | $V_{CC}$-2.0 | | *V* | |
| Power consumption | | 7.0 | | *mW* | 1 Receiver channel, DC |
| | | 20.0 | | *mW* | 1 Transmitter channel |
| | | 115.0 | | *mW* | Total |
| Junction temperature | -25 | 50 | 125 | *°C* | |
| ***LVDS Inputs*** | | | | | |
| Data Rate | 0.0 | | 2.0 | *Gbps* | |
| DC common mode voltage | $V_{EE}$ | | $V_{CC}$ | *V* | DC voltage |
| AC common mode voltage | $V_{EE}$ | | 2.4 | *V* | AC signal <5*MHz* |
| Sensitivity | | 60 | | *mV* | |
| ***CMOS Inputs*** | | | | | |
| Frequency | 0.0 | | 1.0 | *Gbps* | |
| Logic “1” level | $V_{CC}$-0.4 | | | *V* | |
| Logic “0” level | | | 0.4 | *V* | |
| ***LVDS Outputs*** | | | | | |
| Voltage Swing | | 320 | | *mV* | Each SE output |
| CM voltage | 1.2 | | 1.25 | *V* | |
| Impedance | 77 | | 122 | *Ohm* | DC test |
| | 45 | | 115 | *Ohm* | AC test (0-2Gbps) |
| Total current | 5.2 | | 5.7 | *mA* | From “vcc” |
| Output current | 17 | | 27 | *mA* | Shorted to VEE |
| | 4.5 | | 7.0 | *mA* | Shorted together |
| Rise/Fall Times | | TBD | | *pS* | 20%-80% |
| ***CMOS Outputs*** | | | | | |
| Logic “1” level | $V_{CC}$-0.2 | | | *V* | |
| Logic “0” level | | | 0.2 | *V* | |
| Rise/Fall Times | | TBD | | | 20%-to-80% |
| Duty Cycle | 45% | 50% | 55% | | |
| ***CMOS Control Inputs*** | | | | | |
| Logic “1” level | $V_{CC}$-0.4 | | | *V* | |
| Logic “0” level | | | 0.4 | *V* | |

# PACKAGE INFORMATION

The chip is packaged into the standard 40-pin QFN package. The package mechanical information is available on the company’s website.