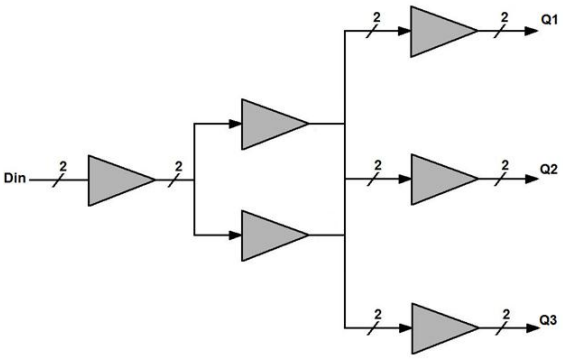
Advanced Science and Novel Technology
27 Via Porto Grande, Rancho Palos Verdes, CA, 90275. Ph. # 1-310-377-6029. Fax # 1-310-377-9940.

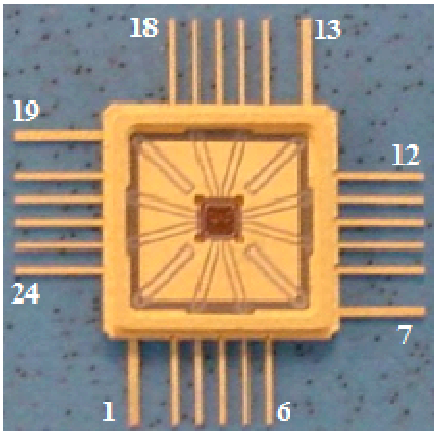
ASNT6112-KMC
25*GHz* 1-to-3 Analog Signal Splitter

- Broadband linear signal splitter for ADC interleaving or similar system applications.
- One input signal port and three phase matched differential output signal ports.
- Greater than 25*GHz* of analog bandwidth.
- Features approximately 0.0*dB* of differential gain.
- Delivers high linearity for differential input signals under 1000*mV* pk-pk.
- Exhibits low jitter and limited temperature variation over industrial temperature range.
- Fully differential input and output buffers with on-chip 50*Ohm* termination.
- Linear output interface with an up to 500*mV* single-ended swing.
- Single ±3.3*V* power supply with 1.35*W* of power consumption.
- Fabricated in SiGe for high performance, yield, and reliability.
- Custom CQFP 24-pin package.

DESCRIPTION



Functional Block Diagram



Package View

The temperature stable ASNT6112-KMC 1-3 analog signal splitter is intended for use in high-speed interleaved ADC or similar systems. The active splitter can receive a broad-band analog signal and effectively distribute it to three separate phase matched differential outputs with on-chip 50*Ohm* termination that provides Vcc-0.55*V* common mode voltage in combination with the required external 50*Ohm* DC loading. The partôs differential input provides an equivalent on-chip 50*Ohm* termination and can be used in either DC or AC coupling modes. In the first mode, the input signalôs common mode voltage should comply with the specifications shown below. In the second mode, the input termination provides the required common mode voltage automatically. The splitterôs I/Os should be used differentially for optimal performance. The IC operates from a single ±3.3*V* power supply.

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Power Supply Configuration

The ASNT6112-KMC can operate with either Vcc = 0.0V and Vee = -3.3V or Vcc = +3.3V and Vee = 0.0V. Different PCB layouts will be needed for each different power supply combination.

All the characteristics detailed below assume Vcc = 0.0*V* and Vee = -3.3*V*.

Absolute Maximum Ratings

Caution: Exceeding the absolute maximum ratings may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground.

Parameter	Min	Max	Units
Supply Voltage - VEE		-3.8	*V*
Power Consumption		1.56	*W*
RF Input Voltage Swing (SE)		1.4	*V*
Operational Temperature	-5	+85	*°C*
Case Temperature		+100	*°C*
Storage Temperature	-40	+100	*°C*
Operational Humidity	10	98	*%*
Storage Humidity	10	98	*%*

TERMINAL FUNCTIONS

TERMINAL NAME	TERMINAL (NO.)	TYPE	DESCRIPTION
vcc	2, 4, 6, 8, 10, 12 14, 16, 18, 20, 22, 24	PS	Power supply: 0*V* (GND)
vee	1, 7, 13, 19	PS	Power supply: -3.3*V*
dp	21	Input	Differential high-speed analog signal inputs
dn	23		
q1p	17	Output	Differential high-speed analog signal outputs
q1n	15		
q2p	11	Output	Differential high-speed analog signal outputs
q2n	9		
q3p	5	Output	Differential high-speed analog signal outputs
q3n	3		

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ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
VEE	-3.1	-3.3	-3.5	V	±6%
VCC		0.0		V	
IEE		410		mA	
Power		1350		mW	
Junction Temp.	0	50	125	°C	
Input (in) Bandwidth		25		GHz	-3 dB
CM Level	-0.6	-0.5	-0.4	V	
Input Noise Density		1.5		nV/sqrt(Hz)	
S11		-10		dB	DC to 30*GHz*
Output (out) CM Level		-0.55		V	
S22		-8		dB	DC to 30*GHz*
Small Signal Differential Gain		0		dB	At 10*GHz*
Output referred 1dB Compression Point		2.7		dBm	Single-Ended, 20*GHz*
THD		0.2		%	Vout=400*mV*p-p,SE

PACKAGE INFORMATION

The chip die is housed in a custom, 24-pin Kyocera metal-ceramic package (CQFP). Kyoceraôs dimensioned drawings are included in this document for reference. The packageôs leads will be trimmed to a length of 1.0mm.

After trimming, the packageôs leads will be further processed as follows:

1. The leadôs gold plating will be removed per the following sections of J-STD-001D:
   - 3.9.1 Solderability
   - 3.2.2 Solder Purity Maintenance
   - 3.9.2 Solderability Maintenance
   - 3.9.3 Gold Removal

2. The leads will be tinned with Sn63Pb37 solder.

It is recommended that the center heat slug located on the back side of the package *not* be soldered to ground or any other potential to help dissipate heat generated by the chip during operation. For PCB information including footprint etc., please reference the packageôs associated Gerber file.

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The partôs identification label is ASNT6112_KMC. The first 8 digits of the name before the underscore identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 digits after the underscore represent the packageôs manufacturer, type, and pin out count.

For ASNT6112_KMC:

- ASNT6112 identifies that the part is an analog splitter
- K represents the fact that it is a Kyocera package
- M stands for metal ceramic
- C means that the package has 24-pins

A date is included in the label of each part. This date allows ADSANTEC to track which parts are from which run lot. The table below gives the lot history of this part and the associated date.

Lot	Date
1	04/10

This device complies with the Restriction of Hazardous Substances (RoHS) per EU 2002/95/EC for all six substances.

REVISION HISTORY

Revision	Date	Changes
1.4	4-2011	Added Figure 2 Added lead trimming and processing info
1.3	3-2011	Added Power Supply Configuration text Revised Absolute Maximums Rating table Revised Package Information section Added PCB information
1.2 Previous release Rev 1.1 1-2011	3-2011	Added Absolute Maximums Rating table Added packaging information Added RoHS compliancy Added revision history table Updated power consumption value