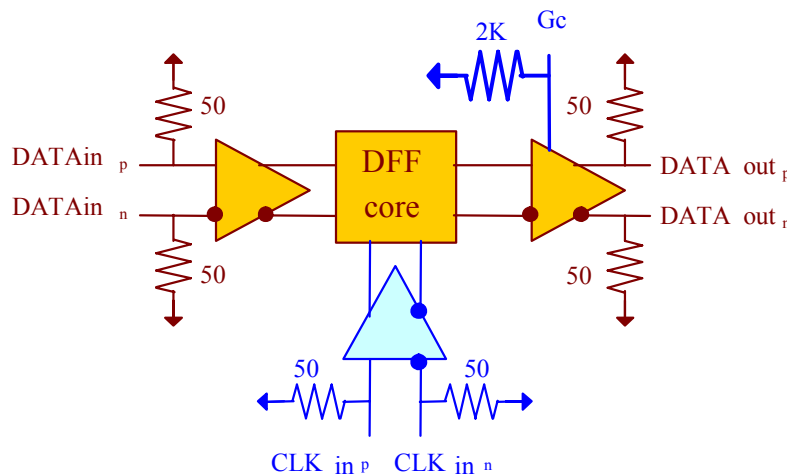
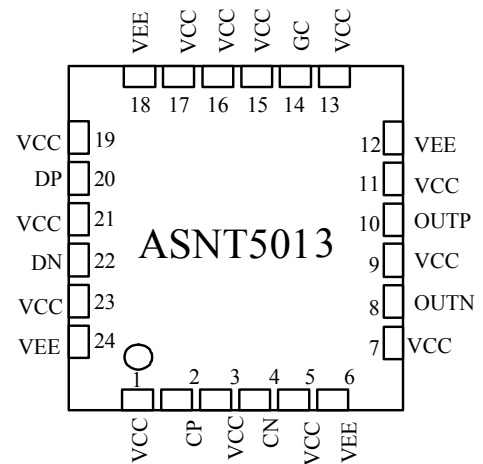


## ASNT5013-PQC 14Gbps D-Type Flip-Flop with Gain Control

- High speed broadband D-Type Flip-Flop for data retiming with full rate clock and single-ended gain control.
- Exhibits low jitter and limited temperature variation over industrial temperature range.
- 14GHz analog input bandwidth for both clock and data inputs.
- 8ps set-up/hold time capability.
- 89% clock phase margin for retiming of data input eye.
- Fully differential input and output buffers with on-chip 50Ω termination.
- CML output interface with variable gain control delivering 0.0V-0.7V single-ended.
- Single -3.3V power supply.
- Power consumption: 510mW.
- Fabricated in SiGe for high performance, yield, and reliability.
- Standard QFN 24-pin package.



Functional Block Diagram



Package Pins

### DESCRIPTION

The temperature stable ASNT5013-PQC SiGe IC provides broadband data retiming with gain control functionality and is intended for use in high-speed measurement / test equipment. ASNT5013-PQC can sample an up to 14Gbps data signal with an up to 14GHz clock source to create a 14Gbps retimed NRZ data with output signal amplitudes between 0.0V-0.7V. The part's I/Os support the CML logic interface with on chip 50Ω termination and may be used differentially, AC/DC coupled, single-ended, or in any combination. It operates from a single -3.3V power supply.



## TERMINAL FUNCTIONS

TERMINAL		TYPE	DESCRIPTION
NAME	(NO.)		
vcc	1,3,5,7,9,11 13,15-17,19,21,23	PS	Power Supply: 0V (GND)
vee	6,12,18,24	PS	Power Supply: -3.3V
dp	20	Input	Differential CML high-speed data signal inputs
dn	22		
cp	2	Input	Differential CML high-speed clock signal inputs
cn	4		
outp	10	Output	Differential CML high-speed data signal outputs
outn	8		
gc	14	Input	Single-ended gain control input

## ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
<b>VEE</b>	-3.1	-3.3	-3.5	V	±6%
<b>VCC</b>		0.0		V	
<b>IEE</b>		155		mA	
<b>Power</b>		510		mW	
<b>Junction Temp.</b>	-25	50	125	°C	
<b>Input Data (d)</b>					
Frequency	0.0		14	Gbps	
CM Level	Vcc-0.8	Vcc-0.3	Vcc+0.3	V	
SE Swing	50	300	800	mV	Peak-to-Peak
<b>Input Clock (c)</b>					
Frequency	0.0		14	GHz	
CM Level	Vcc-0.8	Vcc-0.3	Vcc+0.3	V	
SE Swing	50	300	800	mV	Peak-to-Peak
Duty Cycle	40%	50%	60%		
<b>Output Data (out)</b>					
Frequency	0.0		14	Gbps	
CM Level	Vcc – (half the SE Swing)			V	
SE Swing	0		700	mV	Peak-to-Peak
Rise/Fall Times			<20	ps	20%-80%
Jitter			<10	ps	Peak-to-Peak
Clock Phase Margin	80%	85%	90%		
<b>Tuning Port (gc)</b>					
Control voltage	-1		0	V	

## PACKAGE INFORMATION

The chip is packaged in a standard 24-pin QFN package. The package's mechanical information is available on the company's [website](#).