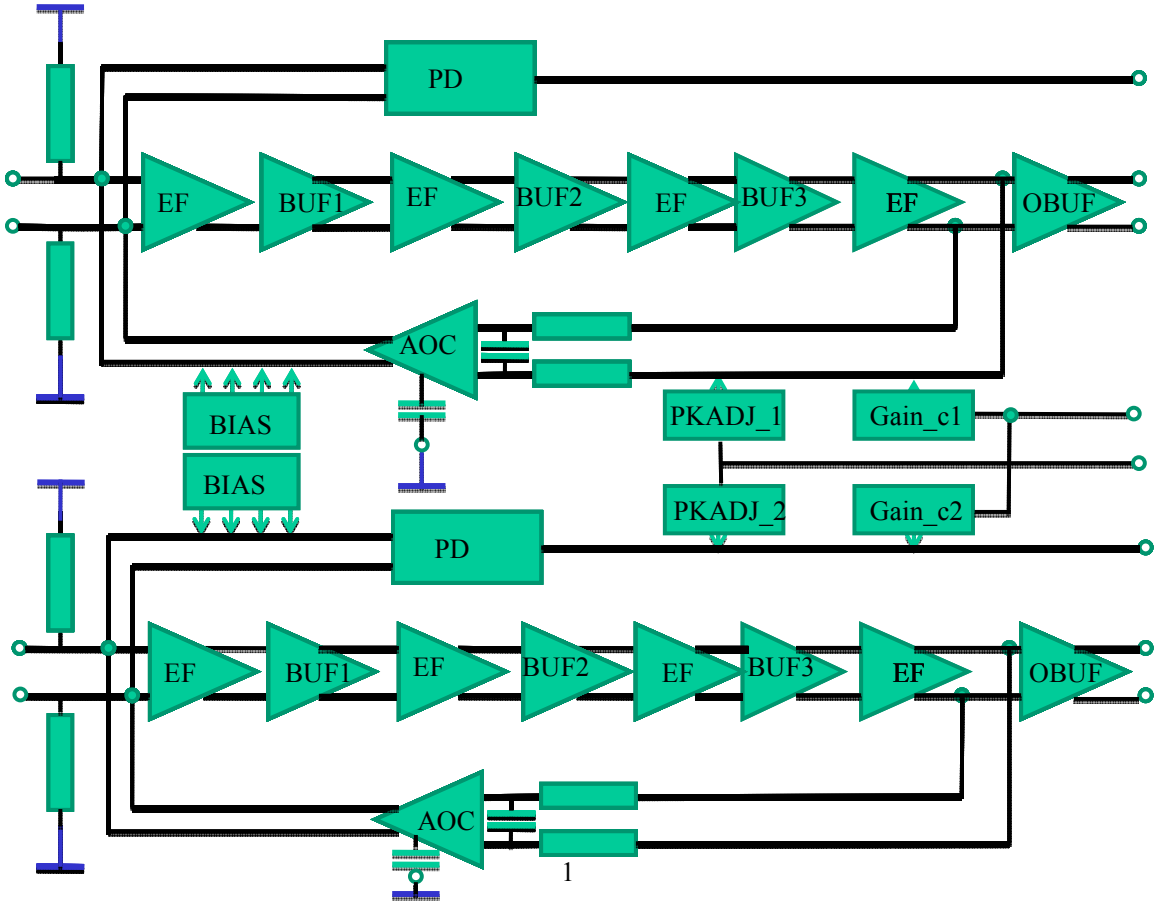
27 Via Porto Grande, Rancho Palos Verdes, CA, 90275. Ph. # 1-310-377-6029. Fax # 1-310-377-9940.

ASNT5138
40G*bps* Dual Limiting Amplifier

- Two parallel broadband limiting amplifiers for receiver side applications.
- Both amplifiers feature automatic input offset control and a peak detector.
- 20*GHz* of analog bandwidth per amplifier channel.
- Adjustable 32-38*dB* of gain for each amplifier.
- Two CML output interfaces with 50Ω termination and 300*mV*p-p single-ended swing.
- Single -3.3*V* power supply.
- Power consumption: 790*mW*.
- Exhibits low jitter and limited temperature variation over industrial temperature range.
- Fabricated in SiGe for high performance, yield, and reliability.

DESCRIPTION



Functional Block Diagram

The temperature stable ASNT5138 SiGe IC provides dual channel low jitter broadband variable signal amplification between its two pair of independent input and output signal ports and is intended for use in high-speed communication systems. ASNT5138 can process two up to 40*Gbps* data signals and deliver two limited 600*mV*p-p differential signals for input signal amplitudes as low as 10*mV*p-p. Automatic offset control (AOC) circuitry is included for both channels to separately adjust each amplifier's unused input signal port when singled ended input signals are applied. AOC's low frequency corner is 10*KHz* with an off chip capacitor value of 300*nF* for both channels. The gain and bandwidth of each amplifier can simultaneously be adjusted through separate external pins. The part's two outputs support the CML logic interface with on chip 50Ω termination and may be used differentially, AC/DC coupled, single-ended, or in any combination. ASNT5138 operates from a single -3.3V power supply.

TERMINAL FUNCTIONS

TERMINAL NAME	(NO.)	TYPE	DESCRIPTION
vcc	7,8,10,12,14,16 18,19,27,28,30 32,34,36,38,39	PS	Power Supply: 0V
vee	1,5,6,13,20 21,25,26,33,40	PS	Power Supply: -3.3V
inp_1	29	Input	High-speed data signal input
inn_1	31	Input	Automatic offset control input
inp_2	35	Input	High-speed data signal input
inn_2	37	Input	Automatic offset control input
outp_1	17	Output	Differential CML high-speed data signal outputs
outn_1	15	Output	
outp_2	11	Output	Differential CML high-speed data signal outputs
outn_2	9	Output	
dca_1	23	Output	300nF off chip capacitor connection
dca_2	3	Output	300nF off chip capacitor connection
pkdet_1	24	Output	Low speed peak detection output
pkdet_2	2	Output	Low speed peak detection output
pkadj	4	Input	Optimum output jitter adjustment
vgc	22	Input	Variable gain control

ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
VEE	-3.1	-3.3	-3.5	V	±6%
VCC		0.0		V	
IEE		240		mA	
Power		790		mW	
Junction Temp.	-25	50	125	°C	
Input (in)					
Frequency	0.0		40	Gb/s	
CM Level	Vcc-0.8	Vcc-0.3	Vcc+0.3	V	
SE Swing	10	200	500	mV	Peak-to-peak

27 Via Porto Grande, Rancho Palos Verdes, CA, 90275. Ph. # 1-310-377-6029. Fax # 1-310-377-9940.

Output (out)					
Frequency	0.0		40	Gb/s	
CM Level		Vcc-0.15		V	
SE Swing	280	300	320	mV	Peak-to-peak
Rise/Fall Times	10	12	14	ps	20%-80%
Additive Jitter			2.0	ps	Peak-to-peak
Tuning Port (vgc)					
Input Signal Range	-1.0		0.0	V	
Gain Variation	32	35	38	dB	< ±5%
Bandwidth	0.0		100	MHz	
Tuning Port (pkadj)					
Input Signal Range	-1.0		0.0	V	
Bandwidth	0.0		100	MHz	
Peak Detect (pkdet)					
Output Signal Range	-1.0		0.0	V	
Bandwidth	0.0		1.0	KHz	