ADSANTEC
Ultra High-Speed Mixed Signal ASICs

Advanced Science And Novel Technology Company, Inc.
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Offices: 310-530-9400 / Fax: 310-530-9402
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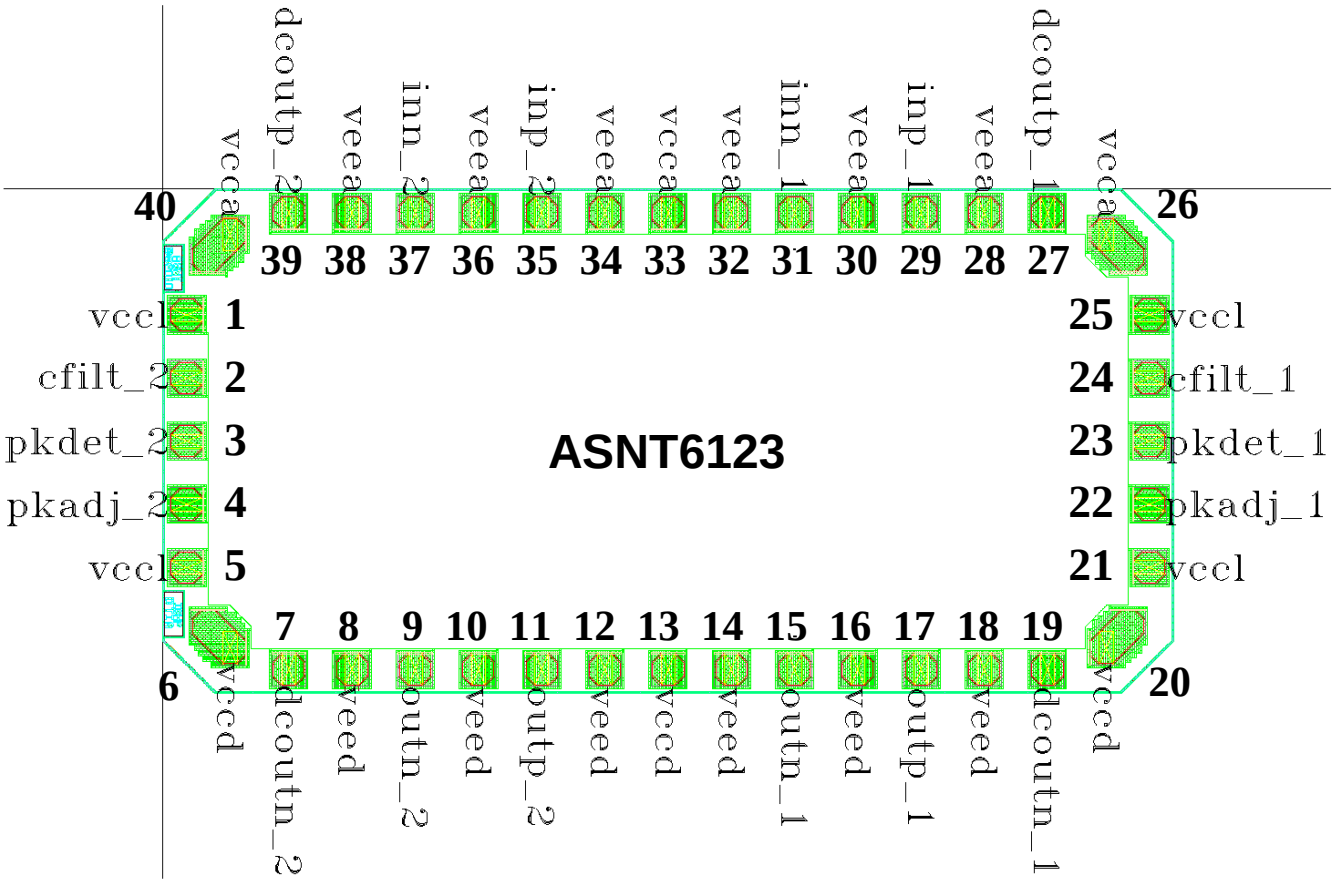
ASNT6123-BD
25*Gbps* Dual TIA

- Broadband dual transimpedance amplifier (TIA) for low noise receiver-side applications
- Two independent amplification channels
- Automatic DC offset adjustment
- Input peak detectors
- Manual bandwidth/peaking adjustment
- Independent common-mode voltage adjustment for each single-ended output
- Exhibits low jitter and limited temperature variation over industrial temperature range
- Fully differential input and output buffers with on-chip 50*Ohm* termination
- Single +3.3*V* or -3.3*V* power supply
- Low current consumption of 150*mA* at nominal conditions
- Fabricated in SiGe for high performance, yield, and reliability



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DESCRIPTION

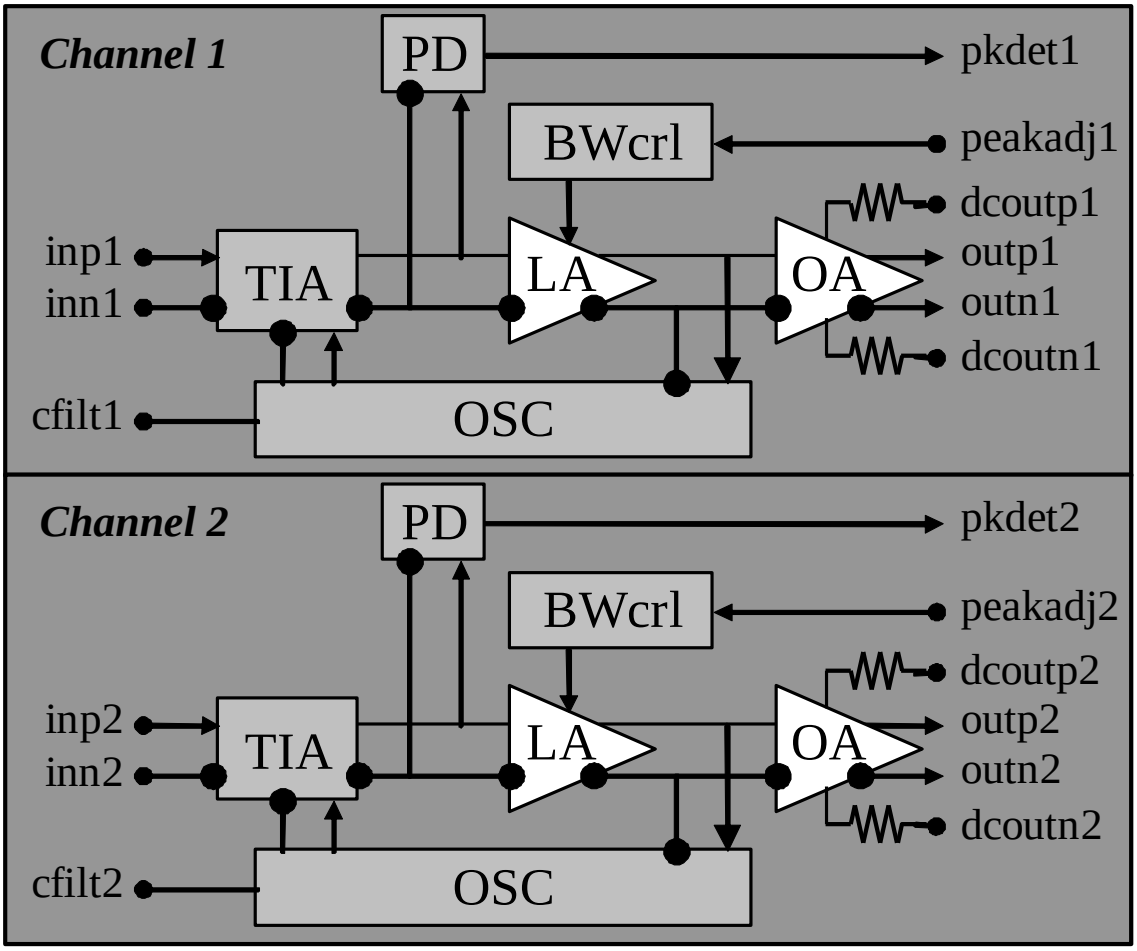

Fig. 1. Functional Block Diagram

The ASNT6123-BD SiGe IC is a two-channel temperature stable SiGe transimpedance amplifier that provides low-jitter broadband linear conversion of current signals at its input ports (inp1/inn1, inp2/inn2) into differential voltage signals at the output ports (outp1/outn1, outp2/outn2). Each channel of the part shown in Fig. 1 is a serial combination of transimpedance (TIA), limiting (LA), and output (OA) amplification stages. The input signal can be either differential or single-ended with the current always flowing into the corresponding pin. In case of one input being single-ended, a certain DC level signal must be applied to the other input. The part incorporates an automatic DC offset control (OSC) that effectively eliminates any difference between the common-mode voltages of direct and inverted output signals. This function requires utilization of external capacitors attached to cfilt1 and cfilt2 pads.

The DC common-mode voltage level of each single-ended output can be manually adjusted using the corresponding dcoutp1/dcoutn1 or dcoutp2/dcoutn2 control inputs.

The individual amplifier bandwidth can be manually adjusted through changing its peaking characteristics by means of peakadj1 or peakadj2 control signals.

The on-chip peak detectors (PD) provide output signals pkdet1 and pkdet2 that are proportional to the values of the corresponding input signals.

The part's outputs support a CML-type interface with on-chip 50*Ohm* termination and may be used as a differential or single-ended connection with AC or DC-coupling (see also POWER SUPPLY CONFIGURATION). The input and output termination resistors in both channels are respectively connected to separate internal positive supply plains vcca and vccd, which may be also kept separate from the intermediate amplifier supply vccl. The input and output negative supply nets are also created as separate metal plains veea and veed, which are partly shorted through the common substrate.

POWER SUPPLY CONFIGURATION

The part can operate with either negative supply (vcca=vccl=vccd=0.0*V*=ground and veea=veed=−3.3*V*), or positive supply (vcca=vccl=vccd=+3.3*V* and veea=veed=0.0*V*=ground). In case of the positive supply, all outputs need AC termination when connected to any devices with 50*Ohm* termination to ground.

The chip substrate should be completely isolated or connected to veea or veed. DO NOT connect substrate to vcca, vccl, or vccd!

All the characteristics detailed below assume vcc = 3.3*V* and vee = 0.0*V*.

ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 1 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground (assumed vee).

Table 1. Absolute Maximum Ratings.

Parameter	Min	Max	Units
Supply Voltage (vcc)		3.6	*V*
Power Consumption		0.6	*W*
RF Input Current Swing (SE)		2	*mA*
Junction Temperature		+125	*ºC*
Storage Temperature	-40	+100	*ºC*
Operational Humidity	10	98	*%*
Storage Humidity	10	98	*%*

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TERMINAL FUNCTIONS

TERMINAL			DESCRIPTION
Name	**No.**	**Type**	
High-Speed I/Os			
inp1	29	Current input	Direct and inverting single-ended current-sensing data inputs for channel 1
inn1	31		
inp2	35		Direct and inverting single-ended current-sensing data inputs for channel 2
inn2	37		
outp1	17	CML output	Differential data outputs for channel 1. Require external SE 50*Ohm* termination to vccd
outn1	15		
outp2	11		Differential data outputs for channel 2. Require external SE 50*Ohm* termination to vccd
outn2	9		
Controls			
dcoutp1	27	Control voltage	DC common-mode voltage control with 1*KOhm* to outp1
dcoutn1	19		DC common-mode voltage control with 1*KOhm* to outn1
dcoutp2	39		DC common-mode voltage control with 1*KOhm* to outp2
dcoutn2	7		DC common-mode voltage control with 1*KOhm* to outn2
pkadj1	22		Channel 1 peaking control signal
pkadj2	4		Channel 2 peaking control signal
pkdet1	23	Analog signal	Channel 1 peak detector output
pkdet2	3		Channel 2 peak detector output
cfilt1	24		300*nF* off-chip capacitor connection for channel 1
cfilt2	2		300*nF* off-chip capacitor connection for channel 2

Supply and Termination Voltages		
Name	**Description**	**Pin Number**
vcca	Positive power supply for TIAs (+3.3*V* or 0*V*)	40, 26, 33
vccl	Positive power supply for internal cells (+3.3*V* or 0*V*)	1, 5, 21, 25
vccd	Positive power supply for output buffers (+3.3*V* or 0*V*)	6, 13, 20
veea	Negative power supply for TIAs (0*V* or -3.3*V*)	28, 30, 32, 34, 36, 38
veed	Negative power supply for other cells (0*V* or -3.3*V*)	8, 10, 12, 14, 16, 18

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ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vcca	3.1	3.3	3.5	*V*	±6%
vccd	3.1	3.3	3.5	*V*	±6%
vccl	3.1	3.3	3.5	*V*	±6%
veea		0.0		*V*	External ground
veed		0.0		*V*	External ground
*I*vee		150		*mA*	Total current from negative supplies
Power consumption		495		*mW*	
Junction temperature	-25	50	125	*°C*	
HS Input Data (inp1/inn1, inp2/inn2)					
Data Rate	DC		25	*Gbps*	
Bandwidth	16		20	*GHz*	-3*dB* level
SE Current Swing			1500	*uA*	Positive (into the pin)
OSC frequency	10			*KHz*	With 300*nF* external capacitor
Input Control Voltages (pkadj1, pkadj2, dcoutp1/dcoutn1, dcoutp2/dcoutn2)					
Frequency		DC			
Logic “0” level		vee		*V*	
Logic “1” level		vcc		*V*	
HS Output Data (outp1/outn1, outp2/outn2)					
Data rate	DC		25	*Gbps*	
Differential gain	77		81	*dBOhm*	
Single-ended swing	0.27		0.32	*V*	Peak-to-peak
CM Level		vcc-(Swing)/2		*V*	With external 50*Ohm* DC termination
Input-referred noise		15	25	$pA/Hz^{1/2}$	0.1*GHz*-20*GHz*
Additive Jitter			2	*ps*	Peak-to-peak

DIE INFORMATION

The main dimensions of the die are given in Table 2.

Table 2. Important Die Dimensions

Pad metal dimensions	80*µm* x 80*µm*
Pad opening dimensions	74*µm* x74*µm*
Die dimensions	1200*µm* x 2400*µm*

The part’s die incorporates wire bonding pads with the coordinates of their centers given in This device *complies with the Restriction of Hazardous Substances (RoHS) per 2011/65/EU for all ten substances.* Table 3.

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The part's identification label is ASNT6123-BD. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 2 characters after the dash indicate that the die is not packaged.

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Table 3. Die Pad Coordinates

Pin Number	X Coordinate, *µm*	Y Coordinate, *µm*	Pin Number	X Coordinate, *µm*	Y Coordinate, *µm*
1	300	58	2	450	58
3	600	58	4	750	58
5	900	58	6	1065	135
7	1142	300	8	1142	450
9	1142	600	10	1142	750
11	1142	900	12	1142	1050
13	1142	1200	14	1142	1350
15	1142	1500	16	1142	1650
17	1142	1800	18	1142	1950
19	1142	2100	20	1065	2265
21	900	2342	22	750	2342
23	600	2342	24	450	2342
25	300	2342	26	135	2265
27	58	2100	28	58	1950
29	58	1800	30	58	1650
31	58	1500	32	58	1350
33	58	1200	34	58	1050
35	58	900	36	58	750
37	58	600	38	58	450
39	58	300	40	135	135

REVISION HISTORY

Revision	Date	Changes
2.3.2	05-2020	Updated Die Information
2.2.2	07-2019	Updated Letterhead
2.2.1	04-2017	Added description of substrate connection Updated absolute maximum ratings section Corrected electrical characteristics section
2.1.1	03-2015	Added gain value
2.0.1	12-2013	Corrected description Corrected format Added die drawing Corrected block diagram Added power supply configuration section Added absolute maximum ratings section Corrected electrical characteristics

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		Added die information Added revision history table
1	01-2010	First release