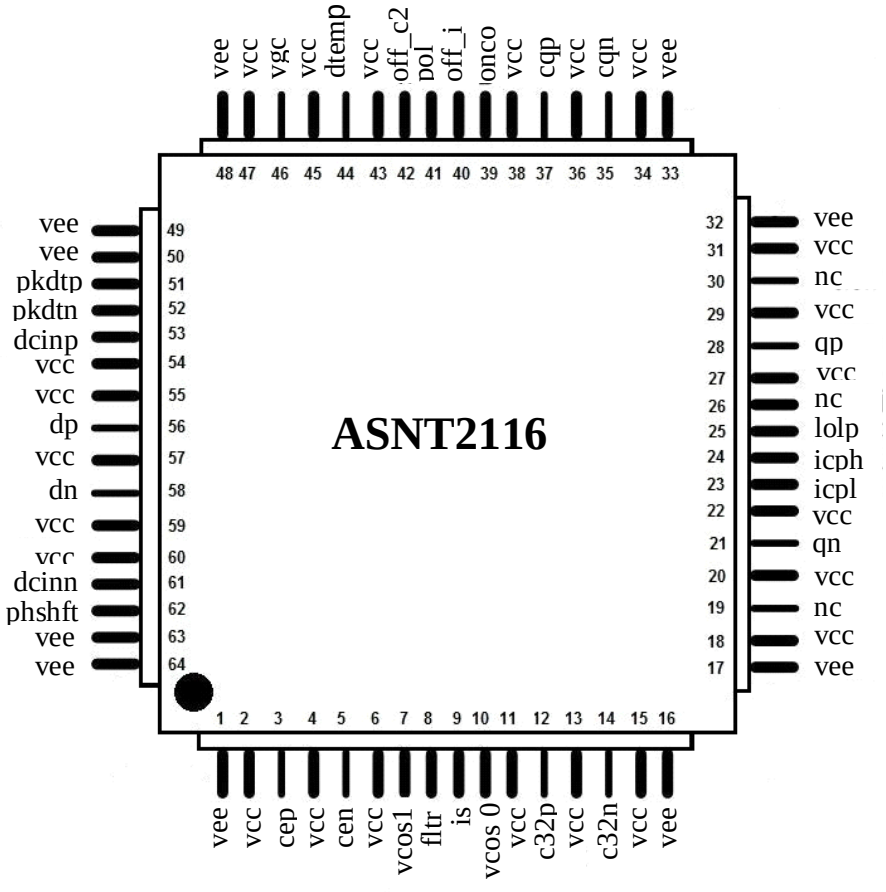
ADSANTEC
Ultra High-Speed Mixed Signal ASICs

Advanced Science And Novel Technology Company, Inc.
2790 Skypark Drive Suite 112, Torrance, CA 90505

Offices: 310-530-9400 / Fax: 310-530-9402
www.adsantec.com

ASNT2116-KMF
25.0-to-31.5*GHz* Programmable CDR 1-to-1

- 1-to-1 CDR (clock and data recovery unit)
- CDR range from 25.0*GHz* to 31.5*GHz* covered by 3 selectable VCOs
- Digital operational mode with DC to 32*GHz* external clock
- RZ and NRZ input data formats
- Adjustable time of the data sampling point for optimal BER performance
- Selectable full-rate, half-rate, or disabled clock output
- Optional signal inversion in all output buffers
- Fully differential CML input and output interfaces for high-speed clock and data
- LVDS-compliant input reference clock interface
- Single +3.3*V* power supply
- Power consumption: 2.25*W* at the maximum operational speed
- Custom CQFP 64-pin package



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DESCRIPTION

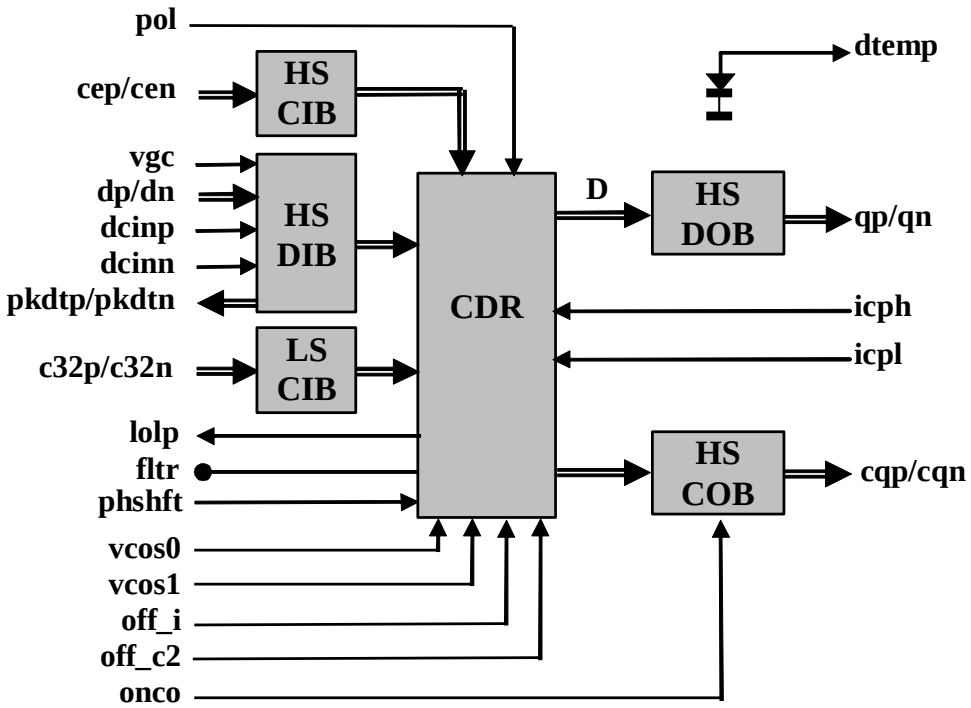

Fig. 1. Functional Block Diagram

ASNT2116-KMF is a 1:1 full-rate clock and data recovery unit (CDR). The main function of the IC shown in Fig. 1 is to recover a full-rate clock signal C and a retimed data signal D from an RZ or NRZ input data signal dp/dn with a bit rate of f_{bit} accepted by a CML input data buffer HS DIB. The IC can function either in CDR mode covering a wide range of input data rates by utilizing its three on-chip VCOs (voltage-controlled oscillators), or in broadband digital mode. Selection of the desired operational mode and the CDR input data rate is accomplished through pins vcos0 and vcos1 (see Table 1). An external low speed reference clock c32p/c32n running at 1/32 of the frequency of the active VCO must be applied to a low-speed LVDS clock input buffer LS CIB in CDR mode. An external full-rate clock cep/cen must be applied to a high speed CML clock input buffer HS CIB in digital mode.

The CDR includes two control loops for latching the correct frequency and phase states and requires a single external loop filter connected to pin fltr. The loops' gain can be tuned independently using control signals icph and icpl. The phase of the clock recovered by the CDR can be adjusted using an external control voltage phshft. This helps achieve the lowest system bit error rate (BER) by selecting the optimal input data sampling time. An internal control circuit generates an alarm signal lolp that indicates the frequency locking state of the CDR.

The data input buffer HS DIB can operate with either differential or single-ended input signals dp/dn. It includes tuning pins dcinp/dcinn for DC offset of the input signals in case of AC termination. When the buffer is operating with a DC-terminated single-ended input signal, a correct threshold voltage should be applied to the unused input pin. A peak detector is also included to provide means of demodulating AM components carried by the input data with a frequency up to a few hundred *kHz*. The peak detector's output signal is delivered to differential port pkdtp/pkdtn.

Depending on the state of control signal off_c2, either a full-rate or a half-rate recovered clock is delivered to outputs cqp/cqn by CML output buffer HS COB. The clock polarity can be inverted using another control signal off_i. The buffer HS COB can be enabled or disabled using control signal onco. The retimed data is delivered to outputs qp/qn by CML output buffer HS DOB. It has a tight phase alignment to output clock cqp/cqn.

All CML I/Os provide on chip 50*Ohm* termination to vcc and may be used differentially, AC/DC coupled, single-ended, or in any combination (see HS DIB). The LVDS input buffer should be used in accordance with the standard (see LS CIB).

The internal temperature can be monitored by a diode's current running into pin dtemp.

HS DIB

The High-Speed Data Input Buffer (HS DIB) can process input data signals dp/dn in either RZ or NRZ format due to its high analog bandwidth. It supports the CML logic interface with on chip 50*Ohm* termination to vcc and may be used differentially, AC/DC coupled, single-ended, or in any combination (see also POWER SUPPLY CONFIGURATION). In the DC-coupling mode, the input signal's common mode voltage should comply with the specifications shown in ELECTRICAL CHARACTERISTICS. In the AC-coupling mode, the input termination provides the required common mode voltage automatically. The differential DC signaling mode is recommended for optimal performance. In case of AC termination, the tuning pins dcinn or dcinp allow for internal data common mode adjustment. This adjustment may be used for changing the slicing level before the data is sampled by the recovered clock. The tuning ports have internal 1*kOhm* single-ended terminations to vcc.

The small-signal gain of the buffer can be adjusted from 32*dB* to 38*dB* using control voltage vgc. The control port has an internal 2*kOhm* termination to vcc. The allowed range is from vee to vcc.

Also included in the buffer is an input signal peak detector that delivers its response through the output differential port pkdtp/pkdetn. The detector can demodulate AM component(s) carried by the input data in the frequency range of up to a few hundred *kHz*. The detector's output ports have internal 2.8*kOhm* single-ended terminations to vcc.

HS CIB

The High-Speed Clock Input Buffer (HS CIB) can process external clock signals cep/cen in the digital operational mode. It supports the CML logic interface with on chip 50*Ohm* termination to vcc and may be used in the same modes as the HS DIB.

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LS CIB

The Low-Speed Clock Input Buffer (LS CIB) can process an external reference clock signal c32p/c32n with a frequency equal to 1/32 of the selected VCO frequency. The clock input supports the LVDS logic interface with on chip 100*Ohm* terminations between the direct and inverted lines. The proprietary LVDS buffer exceeds the requirements of standards IEEE Std. 1596.3-1996 and ANSI/TIA/EIA-644-1995. It is designed to accept differential signals with amplitudes above 70*mV* peak-to-peak (p-p), DC common mode voltage variation between the negative vee and positive vee+2.4*V* supply rails, and AC common mode noise with a frequency up to 5*MHz* within the same voltage range. It can also receive single-ended signals with amplitudes above 60*mV*p-p and threshold voltages between vee and vee+2.4*V*.

CDR

The Clock and Data Recovery block (CDR) contains two loops for adjusting both the phase and the frequency of the internal clock generated by the selected VCO. The frequency loop works in conjunction with the low-speed clock c32p/c32n, while the phase loop utilizes the input data signal dp/dn. The CDR requires an off-chip loop filter with the proposed schematic shown in Fig. 2. The filter should be connected to pin ftr.

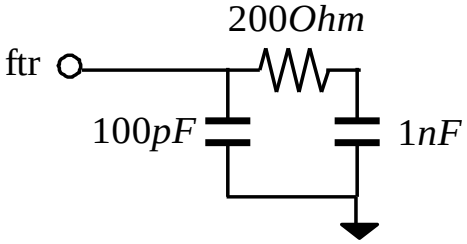

Fig. 2. Proposed External Loop Filter

The main function of the CDR is to frequency-lock the selected on-chip VCO to the input data signal (clock recovery) while aligning the phases in such a way that the incoming data is latched-in with the minimal error (data recovery). By default, the CDR positions the recovered clock's working edge in the middle of the incoming data bits. Using external control voltage phshft with the range from vee to vcc, this edge can be shifted back or forth in order to locate the optimum data sampling point that provides the lowest system BER. The recovered clock is also divided down in frequency by two (C2) and either the full-rate or the half-rate clock is delivered to HS COB depending on the state of the 2.5*V* CMOS control signal off_c2 (off_c2 = "1" (default): full-rate; off_c2 = "0": half-rate).

By utilizing the 2.5*V* CMOS control pins vcos0 and vcos1, the desired working mode and the frequency of the CDR can be selected in accordance with Table 1 below.

The phase and frequency loops' gains can be adjusted by two 2.5*V* CMOS control pins icph and icpl that control the currents in the corresponding sections of the charge pump as shown in Table 2.

Table 1. CDR Mode Selection

vcos0	vcos1	Selected VCO
"0"	"0"	VCO1 (lower frequency)
"0"	"1"	VCO2 (medium frequency)
"1"	"0"	VCO3 (higher frequency)
"1"	"1"	Digital mode, all VCOs disabled (default state)

The lock detect circuitry generates an active-high 2.5*V* CMOS signal lolp that indicates that the frequency difference between the recovered full-rate clock divided by 32 and the applied system reference clock c32p/c32n exceeds ±1000*ppm*.

Table 2. Charge Pump Current Control

icph	icpl	Charge Pump current, *mA*	
		Phase loop section	Frequency loop section
"0"	"0"	550	69
"0"	"1"	550	35
"1"	"0"	275	69
"1"	"1"	275	35

The CDR allows for polarity inversion of the sampled data signal by means of a 2.5*V* CMOS control signal pol (pol = "1" (default): inverted; pol = "0": direct), and of the recovered high-speed clock signal by means of a 2.5*V* CMOS control signal off_i (off_i = "1" (default): direct; off_i = "0": inverted).

HS DOB

The High-Speed Data Output Buffer (HS DOB) receives full-rate retimed serial data stream D from the CDR and converts it into CML output signal qp/qn. This buffer provides internal single-ended 50*Ohm* terminations to vcc for each output line and also requires 50*Ohm* external termination resistors to be connected between vcc and each output.

HS COB

The High-Speed Clock Output Buffer (HS COB) receives a full-rate or a half-rate clock signal from the CDR and converts it into CML output signal cqp/cqn. The buffer provides internal single-ended 50*Ohm* terminations to vcc for each output line and also requires 50*Ohm* external termination resistors to be connected between vcc and each output. The buffer can be enabled or disabled by external 2.5*V* CMOS control signal onco (onco = "1" (default): enabled; onco = "0": disabled). The negative edges of the cqp/cqn signal are aligned to transitions of the output data signal.

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POWER SUPPLY CONFIGURATION

The part operates with a single positive supply (vcc = +3.3*V* and vee = 0.0*V* = ground). All CML I/Os need AC termination when connected to any devices with 50*Ohm* termination to ground.

All the characteristics detailed below assume vcc = 3.3*V* and vee = 0*V* (external ground)

ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 3 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground (assumed vee).

Table 3. Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage (vcc)		3.6	*V*
Power Consumption		2.5	*W*
Input Voltage Swing (SE)		1.0	*V*
Case Temperature		+90	*ºC*
Storage Temperature	-40	+100	*ºC*
Operational Humidity	10	98	*%*
Storage Humidity	10	98	*%*

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TERMINAL FUNCTIONS

TERMINAL			DESCRIPTION
Name	**No.**	**Type**	
High-Speed I/Os			
cep	3	CML Input	Differential full-rate clock inputs with internal SE 50*Ohm* termination to vcc
cen	5		
qp	28	CML Output	Differential full-rate data outputs with internal SE 50*Ohm* termination to vcc. Require external SE 50*Ohm* termination to vcc
qn	21		
cqp	37	CML Output	Differential high-speed clock outputs with internal SE 50*Ohm* termination to vcc. Require external SE 50*Ohm* termination to vcc
cqn	35		
dp	56	CML Input	Differential data inputs with internal SE 50*Ohm* termination to vcc
dn	58		
Low-Speed I/Os			
c32p	12	LVDS Input	Differential low-speed clock input with internal differential 100*Ohm* termination
c32n	14		
pkdtp	51	Output	Peak detector outputs with internal SE 2.8*KOhm* termination to vcc
pkdtn	52		
Digital Controls			
vcos1	7	2.5*V* CMOS Input	CDR operational mode and VCO frequency selection, see Table 1
vcos0	10		
is	9		VCO current control (high, default: higher current; low: lower current) For test purposes only! Keep not connected for normal operation!
icpl	23		Charge pump current control, see Table 2
icph	24		
onco	39		COB control (high, default: buffer is enabled; low: buffer is disabled)
off_i	40		Output clock polarity (high, default: direct; low: inverted)
pol	41		Output data polarity (high, default: inverted; low: direct)
off_c2	42		Output clock select (high, default: buffer is on; low: buffer is disabled)
lolp	25	2.5*V* CMOS	CDR lock indicator output (high: no lock; low: locked)
Control Voltages			
fltr	8	Input	External loop filter connection
vgc	46	Input	Input gain control voltage. Allowed values from vee to vcc
dcinp	53	DC Input	Input data common mode voltage adjustment. Allowed values from vee to vcc
dcinn	61		
phshft	62	DC Input	CDR sampling point adjustment. Allowed values from vee to vcc
dtemp	44	Output	On-chip temperature control diode's anode

Supply and Termination Voltages		
Name	**Description**	**Pin Number**
vcc	Positive power supply (+3.3*V*)	2, 4, 6, 11, 13, 15, 18, 20, 22, 27, 29, 31, 34, 36, 38, 43, 45, 47, 54, 55, 57, 59, 60
vee	Negative power supply (0*V*)	1, 16, 17, 32, 33, 48, 49, 50, 63, 64
nc	Not connected pins	19, 26, 30

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ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vee		0.0		*V*	External ground
vcc	3.1	3.3	3.5	*V*	±6%
*I*vcc		680		*mA*	
Power consumption		2.25		*W*	
Junction temperature	-25	50	125	*°C*	
Package t° resistance		15		*°C/W*	
HS Input Data (dp/dn)					
Data Rate	25.0		31.5	*Gbps*	RZ or NRZ, CDR mode
	DC		32	*Gbps*	RZ or NRZ, digital mode
Swing	0.05		0.6	*V*	Differential or SE, p-p
External CM voltage	vcc-0.8		vcc	*V*	Must match for both inputs
Internal CM voltage	vcc-0.15		vcc	*V*	Set by dcinp/dcinn on the corresponding inputs
HS DIB gain	32		38	*dB*	Controlled by vgc
HS Input Clock (cep/cen)					
Frequency	DC		32	*GHz*	
Swing	0.05		0.6	*V*	Differential or SE, p-p
CM voltage level	vcc-0.8		vcc	*V*	Must match for both inputs
Duty Cycle	45	50	55	*%*	
LS Input Reference Clock (c32p/c32n)					
Frequency	781.25		984.38	*MHz*	1/32 of the VCO frequency
Swing	140		900	*mV*	Differential, p-p
CM voltage level	vee		vee+2.4	*V*	
Duty cycle	40	50	60	*%*	
HS Output Data (qp/qn)					
Data rate	DC		32	*Gbps*	NRZ
Logic “1” level		vcc		*V*	
Logic “0” level		vcc -0.4		*V*	
Jitter		8		*ps*	p-p at 25.6*Gbps*
HS Output Clock (cqp/cqn)					
Frequency	DC		32	*GHz*	
Logic “1” level		vcc		*V*	
Logic “0” level		vcc -0.4		*V*	
Jitter		5		*ps*	p-p at 12.8*GHz*
Input Data Common Mode Control (dcinp/dcinn)					
Internal termination		1		*kOhm*	SE to vcc
DC voltage range	vee		vcc	*V*	vee creates max downshift
Peak Detector Output (pkdtp/pkdtn)					
Internal termination		2.8		*kOhm*	SE to vcc
Swing p-p (Diff)	-1		1	*V*	Over full input range
CM Voltage Level		vcc -1.0		*V*	

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PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Data Sampling Point Adjustment (phshft)					
Internal termination		1.8		*kOhm*	SE to vcc
Input DC Voltage	vcc -1.0		vcc	*V*	
Phase Shift	-15	0	+15	*ps*	0 at phshft=n/c
Shift Stability	-2		2	ps	From 0°*C* to 125°*C*
Bandwidth	0.0		100	*MHz*	
Input Gain Control (vgc)					
Internal termination		2.0		*kOhm*	SE to vcc
Input DC Voltage	vee		vcc	*V*	vee delivers min gain
CMOS Control I/Os (icph, icpl, vcos0, vcos1, off_i, off_c2, pol, onco, is, lolp)					
Logic "1" level	2.1		2.5	*V*	
Logic "0" level			vee +0.4	*V*	
Timing Parameters					
cqp/cqn to qp/qn delay variation		2		*ps*	Over the full temperature range
VCOs					
Low frequency of VCO1		25.0		*GHz*	Lower-frequency VCO
High frequency of VCO1		27.4		*GHz*	
Low frequency of VCO2		26.3		*GHz*	Medium-frequency VCO
High frequency of VCO2		29.2		*GHz*	
Low frequency of VCO3		28.0		*GHz*	Higher-frequency VCO
High frequency of VCO3		31.5		*GHz*	
External control voltage range (applied to fltr)	vcc-2.5		vcc	*V*	In the open-loop mode
Temperature Monitoring Diode (dtemp)					
Input current		2.33		*mA*	At -25°*C*
		2.48		*mA*	At 125°*C*

PACKAGE INFORMATION

The chip die is housed in a custom 64-pin CQFP package shown in Fig. 3. The package provides a center heat slug located on its back side to be used for heat dissipation. ADSANTEC recommends for this section to be soldered to the vcc plain, which is power for a positive supply.

The part's identification label is ASNT2116-KMF. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package's manufacturer, type, and pin out count.

This device complies with the Restriction of Hazardous Substances (RoHS) per 2011/65/EU for all ten substances.

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64-PIN KMF Package

All Dimensions are in millimeters

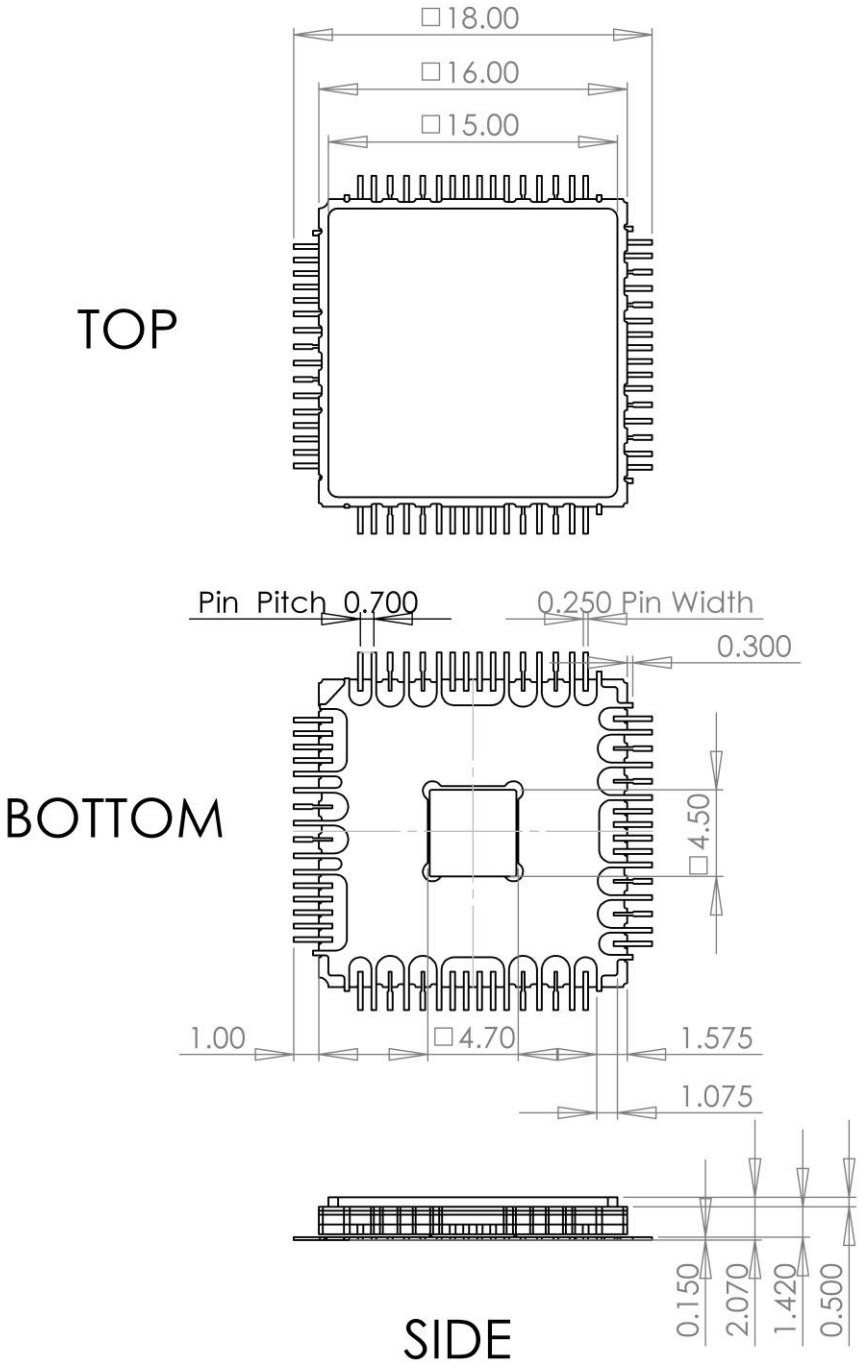

Fig. 3. CQFP 64-Pin Package Drawing (All Dimensions in mm)

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REVISION HISTORY

Revision	Date	Changes
1.4.2	01-2020	Updated Package Information
1.3.2	07-2019	Updated Letterhead
1.3.1	05-2015	Revised package information section
1.2.1	03-2014	Corrected CDR Frequency operating range Corrected Electrical Characteristics
1.1.1	07-2013	Corrected CDR Frequency operating range
1.0.1	05-2013	Initial release