

# **LUCEO** Electrical BERT Module

### PN L-6001-EBERT-3

#### DESCRIPTION

EBERT is a Bit Error Rate Test module that plugs in to the XBERT and ParalleX™ Chassis. EBERT-3 can generate and receive electrical data from 9.9 Gb/s up to 11.3 Gb/s. Optionally the EBERT-3 module can operate at 4.9 Gb/s up to 5.7 Gb/s. User programmable PRBS patterns can be changed via an easy to use GUI. A pattern trigger output provides an electrical trigger synchronous with the pattern for use with an oscilloscope or other test equipment. Optional Pre-emphasis (option 108) applies frequency selective attenuation to the data signal at the transmit side to compensate for losses in the transmit medium. Front panel indicators give immediate status for Tx and Rx Data.

#### **KEY FEATURES**

- Data Rates 9.9 to 11.3 Gb/s. Optional 4.9 to 5.7 Gb/s operation (additional CDR module may be necessary for 4.9-5.7G operation, dependant on device under test)
- Protocol independent OC192, Ethernet, Fibrechannel, Infiniband, 40Gbase, 100Gbase testing
- Test XFP, QSFP, SFP+, TOSA/ROSA, AOC, and other devices
- Differential Electrical Pattern Generator (SMA Connector)
- Differential Electrical Error Detector (SMA Connector)
- 10GHz Clock Output (single ended)
- PRBS: 7, 9, 10, 11, 15, 21, 23, 31

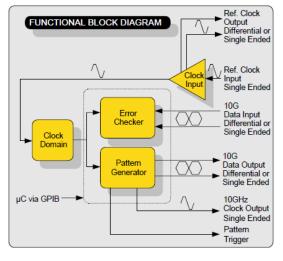
User-Pattern: 8Bit - 8Kbyte Clock-Pattern:  $\frac{1}{1}, \frac{1}{2}, \frac{1}{4}, \frac{1}{8}$ 

Additional: K28.0-K28.7, CJPAT, SSPS-64 and oth

- Duo-Binary pre-coder
- Optional Pre-emphasis of transmit signal
- Data output polarity swap and data input polarity swap
- BER detection: 0.5 to < 10E-15
- Single error and error rate injection: E-3 to E-15
- Data log Gating-time: up to 5000h
- Reference Clock Input (single ended) and output (diff)
- LabView<sup>TM</sup> drivers available
- Small size: width 50.8mm (2")



ELECTRICAL BERT MODULE PN L-6001-EBERT-3



#### XBERT PLATFORM: LETS YOU START SMALL AND GROW BIG

XBERT is a low-cost, modular Bit Error Rate Test Platform used for verification and test of 10Gb/s and above optical and electrical chip, sub assembly and system designs. ParalleX™ allows users to perform several BER tests at once using a single clock source. The system is ideal for developers desiring to run simultaneous BER tests on parallel interfaces or multiple independent interfaces. XBERT and ParalleX™ are scalable so users can start off with a single channel and add modules to grow the system. Manufacturers can realize great savings by taking advantage of the XBERT and ParalleX™ system's scalability to perform parallel testing in volume production environments.



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#### KEY PERFORMANCE PARAMETERS

| PARAMETER   | SYMBOL                          | Min             | Max   | UNIT      | NOTE                          |
|---|---------------------------------|-----------------|-------|-----------|-------------------------------|
| Data Rate   | DR                              | 9.5             | 11.5  | Gbps      | Standard mode                 |
|   |                                 | 4.9             | 5.7   | Gbps      | Additionally by<br>Option 107 |
| Data Formats  |                                 | NRZ, Duo Binary |       |           | Note 4                        |
| Data Output Signal Channel P or N (single ended)  | D <sub>OutP/N</sub>             | 400             | 600   | $mV_{pp}$ |                               |
| Synthesized 10GHz Output Clock (single ended)   | CLK <sub>Out</sub>              | 400             | 1200  | $mV_{pp}$ | f=REFCLK x 16                 |
| Data Output Rise and Fall time  | t <sub>r</sub> / t <sub>f</sub> | Typica          | l 23  | ps        | 20% - 80%                     |
| Output Jitter   | $J_{rms}$                       | Typica          | l 1.1 | ps        | Note 3                        |
| Differential Output Impedance   | Z <sub>ODiff</sub>              | 90              | 110   | Ω         |                               |
| Data Output Termination   |                                 | AC - coupled    |       |           |                               |
| Data Input Signal Channel P or N  | D <sub>InP/N</sub>              | 110             | 700   | $mV_{pp}$ | Single ended                  |
| Differential Data Input signal (D <sub>InDiff</sub> =D <sub>InP</sub> -D <sub>InN</sub> ) | D <sub>InDiff</sub>             | 220             | 1400  | $mV_{pp}$ | Note 1                        |
| Differential Input Impedance  | $Z_{InDiff}$                    | 90              | 110   | Ω         |                               |
| Data Input Termination  |                                 | AC - coupled    |       |           |                               |
| Reference Clock Input Frequency   | P <sub>ref</sub>                | 622.08          | 707.5 | MHz       |                               |
| Reference Clock Input Impedance   | Z <sub>Ref</sub>                | 45              | 55    | Ω         |                               |
| Reference Clock Input Termination   |                                 | AC - coupled    |       |           |                               |
| Sync Signal output amplitude  | Sync                            | 550             | 1100  | mV        | Note 2                        |
| Operating Temperature   | T <sub>OP</sub>                 | 0               | 40    | °C        | Ambient temp.                 |

### Note:

Minimum input voltage to guarantee error free detection (BER  $< 10^{-15}$ )

Default function is pattern trigger. Other functions like pulse per error byte are possible. For more detailed information 2

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contact Luceo Technologies.

Measured at: duty cycle 50%, PRBS31, DR=11.3Gbps

Duo-binary precoder function is a feature of the generator part of the EBERT module. To measure the BER of a duo binary signal it has to be decoded by the user. The duo-binary precoder function can be switched on/off via

Pre-emphasis function (option 108) can be adjusted in 22 steps via GPIB commands or GUI.

