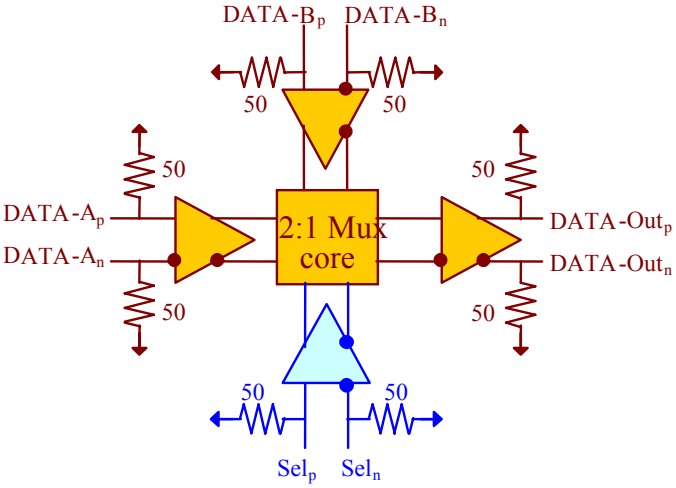
27 Via Porto Grande, Rancho Palos Verdes, CA, 90275. Ph. # 1-310-377-6029. Fax # 1-310-377-9940.

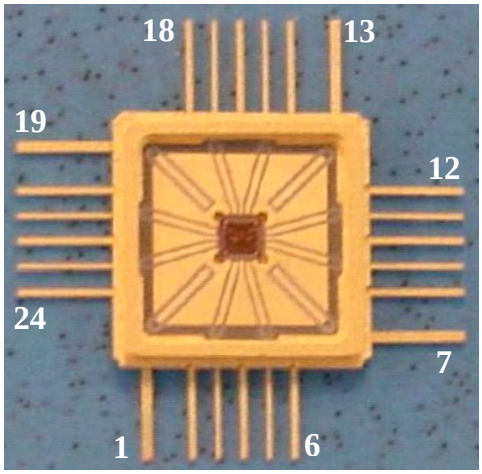
ASNT5050-KMC
30*Gbps* 2:1 Multiplexer

- High speed broadband 2:1 Multiplexer/Selector (MUX) gate.
- Exhibits low jitter and limited temperature variation over industrial temperature range.
- 15*GHz* analog input bandwidth for both data inputs and clock input.
- Ideal for use as a high isolation selector switch or as a high speed 2:1 MUX.
- Ideal for high speed proof-of-concept prototyping.
- Fully differential input and output buffers with on-chip 50Ω termination.
- CML output interface with 400*mV* single-ended swing.
- Single -3.3*V* power supply.
- Power consumption: 450*mW*.
- Fabricated in SiGe for high performance, yield, and reliability.
- Custom CQFP 24-pin package.

DESCRIPTION



Functional Block Diagram



Package View

The temperature stable and broadband ASNT5050-KMC SiGe IC can be utilized as either a high isolation selector switch or a high speed 2:1 multiplexer (MUX) and is intended for use in high-speed measurement / test equipment. When employed as a selector switch, ASNT5050-KMC can route one of its up to 30*Gbps* data inputs to its output while effectively blocking the other data input. Selection of a specific data input is achieved through appropriate external biasing of the selector signal inputs. As a 2:1 MUX, ASNT5050-KMC can receive up to 15*Gbps* input data signals and effectively multiplex them into a 30*Gbps* NRZ output data signal by using an input 15*GHz* clock signal on its selector signal inputs. The part's I/Os support the CML logic interface with on chip 50Ω termination and may be used differentially, AC/DC coupled, single-ended, or in any combination. It operates from a single -3.3V power supply.

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TERMINAL FUNCTIONS

vcc vee	2,4,6,8,10,12 14,16,18,20,22,24 1,7,13,19	PS PS	Power Supply: 0V Power Supply: -3.3V
dbp dbn	21 23	Input	Differential CML high-speed data signal inputs
dap dan	17 15	Input	Differential CML high-speed data signal inputs
selp seln	3 5	Input	Differential CML high-speed clock signal inputs
outp outn	11 9	Output	Differential CML high-speed data signal outputs

ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
VEE	-3.1	-3.3	-3.5	V	±6%
VCC		0.0		V	
IEE		135		mA	
Power		450		mW	
Junction Temp.	-25	50	125	°C	
Input Datas (d)					
Frequency	0.0		30	Gbps	
CM Level	Vcc-0.8	Vcc-0.3	Vcc+0.3	V	
SE Swing	50	300	800	mV	Peak-to-Peak
Input Clock (sel)					
Frequency	0.0		15	GHz	
CM Level	Vcc-0.8	Vcc-0.3	Vcc+0.3	V	
SE Swing	50	300	800	mV	Peak-to-Peak
Duty Cycle	40%	50%	60%		
Output Data (out)					
Frequency	0.0		30	Gbps	
CM Level	Vcc-0.3	Vcc-0.2	Vcc-0.1	V	
SE Swing	380	400	420	mV	Peak-to-Peak
Rise/Fall Times	7	9	11	ps	20%-80%
Additive Jitter			<1	ps	Peak-to-Peak

PACKAGE INFORMATION

The chip is packaged in ADSANTEC's custom 24-pin metal-ceramic package (CQFP). The package's mechanical information is available on the company's website.