ADSANTEC
Ultra High-Speed Mixed Signal ASICs

Advanced Sience And Novel Technologies Company, Inc.
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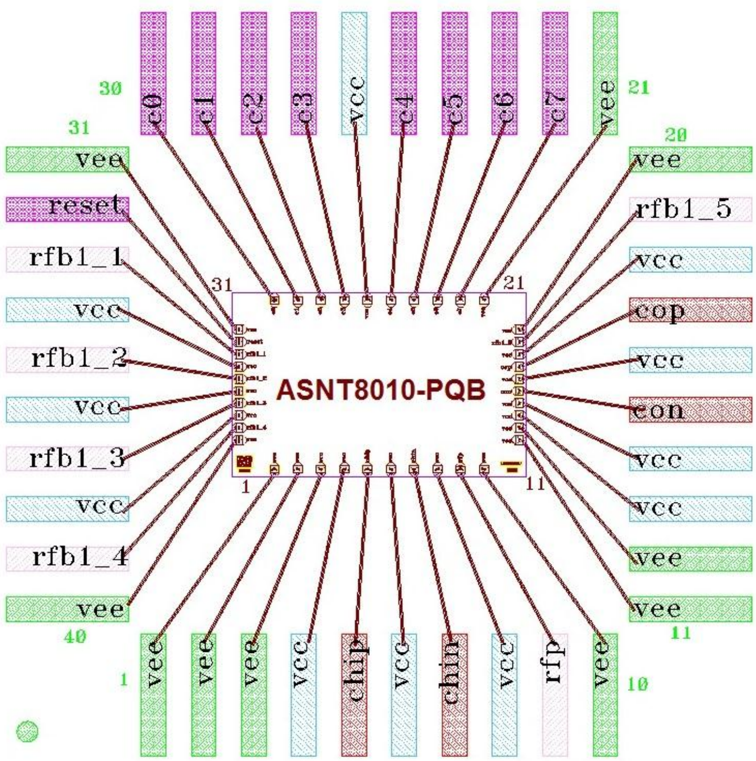
ASNT8010-PQB
17*GHz* Programmable Integer Divider

- Wide frequency range from DC to 17*GHz*.
- Contiguous division ratios from 1 to 256.
- 50% duty cycle of the divided clock signal.
- Differential or single-ended CML input interface with on-chip 50*ohm* termination to the positive supply rail (“vcc”).
- Differential or single-ended CML output interface with on-chip 50*ohm* termination to the positive supply rail (“vcc”).
- Easy 8-bit parallel programming interface compatible with LVTTL or 3.3*V* CMOS standards.
- Optional external reset function.
- Optional dynamic mode of the division ratio adjustment with a short set-up time (about 20*ns* after the pulse edge on any control input).
- Single 2.5...3.5*V* power supply.
- Industrial temperature range.
- Current consumption of 950*mA* at full operational speed.
- Standard 40-pin QFN package with a thermal pad.



PACKAGE DIAGRAM

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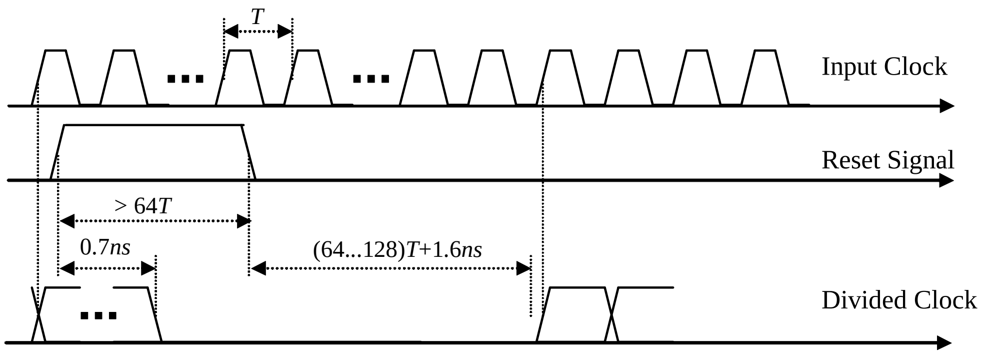
DESCRIPTION

ASNT8010-PQB is a high-speed programmable integer clock divider with static or dynamic adjustment of the division ratio through the standard 8-bit parallel LVTTL/CMOS interface and optional external reset (active-high 3.3*V* CMOS/LVTTL signal). The device automatically resets itself after the initial power-up and any change of the division control signals. When optional external reset signal ("reset") is set to "high", ASNT8010-PQB switches to idle (static "0" output) after a 0.7*ns* delay as shown in the timing diagram below. When "reset" returns to "low", the divider switches back to normal operation after (64...128) periods of the high-speed system clock plus additional 1.6*ns* delay. The minimum allowed "reset" pulse must not be shorter than 64 periods of the high-speed system clock.



The divider accepts the input clock signal ("chip/chin") with a speed from DC to 17*GHz* and provides a clean 50% duty cycle output signal ("cop/con") in any operational mode. The utilized input and output buffers are fully compatible with the CML interface. They feature internal 50*Ohm* termination to the positive supply rail ("vcc") and support both differential (DC or AC) and single-ended (AC) termination modes. The external transmission media can be a printed circuit board or copper coaxial cables with a 50*Ohm* impedance.

The divider allows for both static and dynamic adjustment of the division ratio from 1 to 256 with a step of 1. In the static mode, the binary code on the control inputs "C0"-"C7" defines the value of the ratio from 1 to 255, where "C7" is the most significant bit. All "0"s ("low" state) define the division by 256. Following any change of a control signal in the dynamic mode, the divider switches to idle after (64...128) periods of the high-speed system clock plus additional 1.6*ns* delay, and returns back to normal operation with the new division ratio after additional delay equal to 192 periods of the high-speed system clock.

The chip uses a positive 3.3*V* power supply with "vee" as a ground node and is characterized for operation at −25°C to 125°C of junction temperatures. It can also operate from a negative 3.3V supply voltage with "vcc" as a ground node and the appropriate correction of the control signals.

The device is packaged into a standard 40-pin QFN plastic package with a bottom thermal pad.

APPLICATION

ASNT8010-PQB can be used as a general-purpose reprogrammable divider in a variety of high-frequency synthesizer applications. It is particularly suitable for the advanced measurement equipment.

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PIN-OUT

Pin #	Name	Function	Pin #	Name	Function
1	vee	Negative supply node	21	vee	Negative supply node
2	vee	Negative supply node	22	C7	Division control (MSB)
3	vee	Negative supply node	23	C6	Division control
4	vcc	Positive supply node	24	C5	Division control
5	clkip	Direct clock input	25	C4	Division control
6	vcc	Positive supply node	26	vcc	Positive supply node
7	clkin	Inverted clock input	27	C3	Division control
8	vcc	Positive supply node	28	C2	Division control
9	dec	47nF external capacitor to vee	29	C1	Division control
10	vee	Negative supply node	30	C0	Division control (LSB)
11	vee	Negative supply node	31	vee	Negative supply node
12	vee	Negative supply node	32	res	External reset input
13	vcc	Positive supply node	33	n/c	Keep open!
14	vcc	Positive supply node	34	vcc	Positive supply node
15	clkon	Inverted divided clock output	35	n/c	Keep open!
16	vcc	Positive supply node	36	vcc	Positive supply node
17	clkop	Direct divided clock output	37	n/c	Keep open!
18	vcc	Positive supply node	38	vcc	Positive supply node
19	n/c	Keep open!	39	n/c	Keep open!
20	vee	Negative supply node	40	vee	Negative supply node

PCB DESIGN RECOMMIDATIONS

1. The divider requires a 50*Ohm* impedance environment for clock input and output signals.
2. Pins No. 19, 33, 35, 37, and 39 must be kept OPEN (not connected)!
3. One external capacitor of 47nF must be inserted between pin No. 9 and the ground plane.
4. Additional heat sink is recommended for the reliable operation.

PACKAGE INFORMATION

The chip is packaged in a standard 40-pin QFN package. The package's mechanical information is available on the company's website.