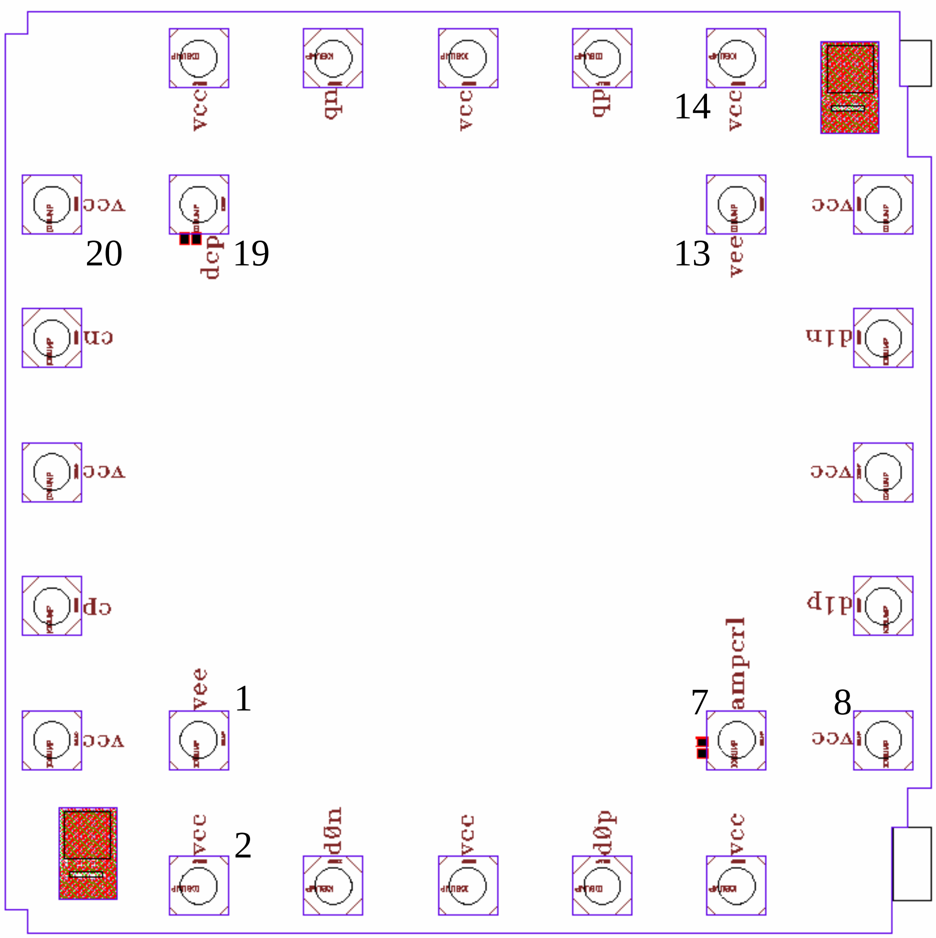
ADSANTEC
Ultra High-Speed Mixed Signal ASICs

Advanced Science And Novel Technology Company, Inc.
2790 Skypark Drive Suite 112, Torrance, CA 90505

Offices: 310-530-9400 / Fax: 310-530-9402
www.adsantec.com

ASNT5650-BD
DC-112*Gbps* Broadband Digital 2:1 Multiplexer/Selector

- High speed broadband 2:1 Multiplexer/Selector (MUX)
- Exhibits low jitter and limited temperature variation over industrial temperature range
- Ideal for use as a high isolation selector switch or as a high speed 2-to-1 serializer
- Fully differential CML input interface
- Fully differential CML output interface
- Adjustable output swing up to 750*mV* single-ended
- Analog input clock common mode voltage control
- Single +3.3*V* or -3.3*V* power supply
- Power consumption: up to 810*mW*
- Fabricated in SiGe for high performance, yield, and reliability



DESCRIPTION

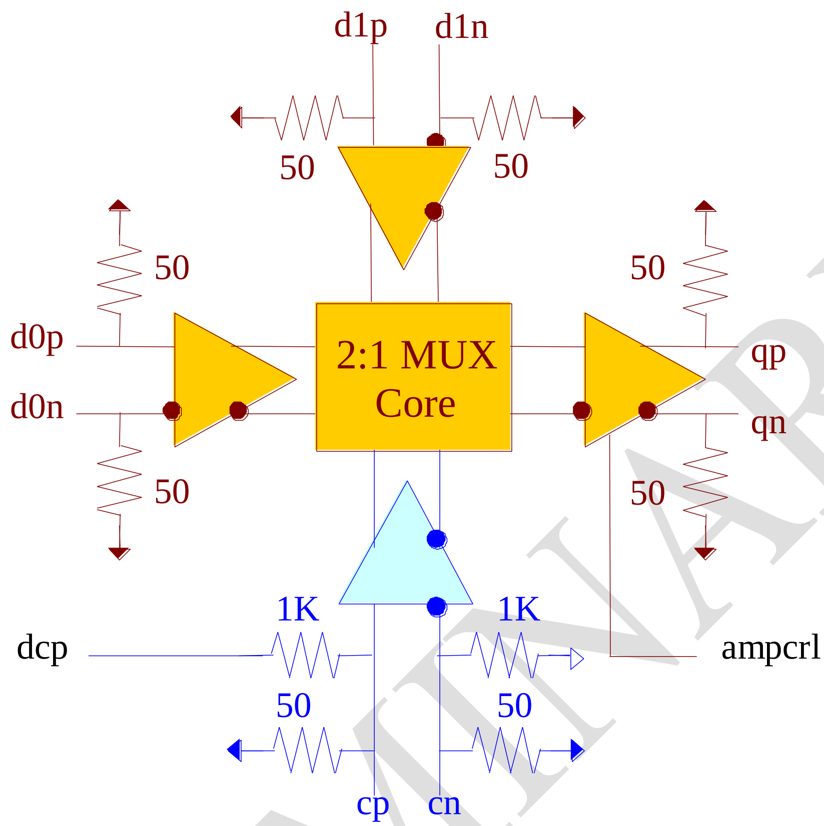


Fig. 1. Functional Block Diagram

The IC shown in Fig. 1 can be utilized as either a high isolation selector switch or a high speed 2:1 serializer and is intended for use in high-speed measurement / test equipment. When employed as a selector switch, the IC can route one of its differential data input signals d0p/d0n or d1p/d1n to its differential output qp/qn while effectively blocking the other data input. Selection of a specific data input is achieved through appropriate external DC biasing of the selector signal inputs cp/cn. The logic is shown in Table 1.

Table 1. Truth Table

c	d0	d1	out
0	X	0	0
0	X	1	1
1	0	X	0
1	1	X	1

As a 2:1 serializer, the IC can receive high speed input data signals into d0p/d0n and d1p/d1n and effectively multiplex them into a double frequency rate NRZ output data signal by using a high speed input clock signal on its selector signal inputs cp/cn. The signals should be aligned as shown in Fig. 2. To ensure both maximum timing margins and low output signal jitter, limit the amount of jitter on the input signals (D0, D1, and C) to only a few picoseconds.

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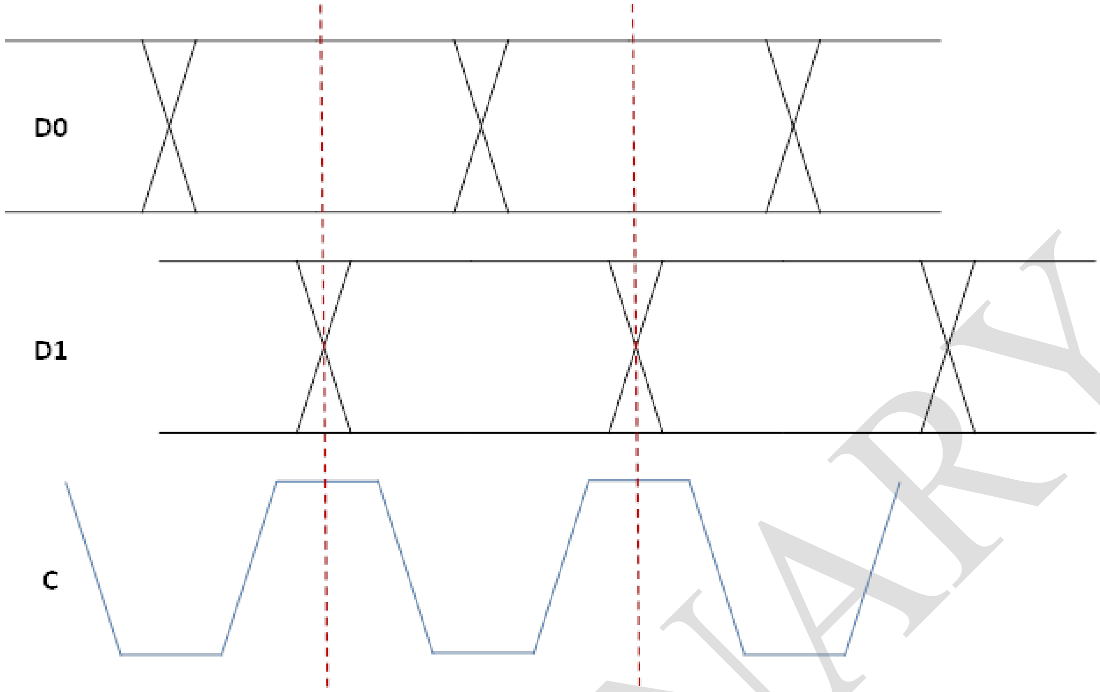

Fig. 2. Input Signal Timing Diagram

The common-mode voltage levels of the input clock signals can be adjusted using an external analog control voltage applied to the port dcp.

The output data swing is controlled by an external analog control voltage applied to the port ampcrl.

The part's I/O's support the CML logic interface with on chip 50*Ohm* termination to vcc and may be used differentially, AC/DC coupled, single-ended, or in any combination (see also POWER SUPPLY CONFIGURATION). In the DC-coupling mode, the input signal's common mode voltage should comply with the specifications shown in ELECTRICAL CHARACTERISTICS. In the AC-coupling mode, the input termination provides the required common mode voltage automatically. The differential DC signaling mode is recommended for optimal performance.

POWER SUPPLY CONFIGURATION

The part can operate with either negative supply (vcc = 0.0*V* = ground and vee = −3.3*V*), or positive supply (vcc = +3.3*V* and vee = 0.0*V* = ground). In case of the positive supply, all I/Os need AC termination when connected to any devices with 50*Ohm* termination to ground.

All the characteristics detailed below assume vcc = 0.0*V* and vee = -3.3*V*.

ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 2 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All max voltage limits are referenced to ground.

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Table 2. Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage (vee)		-3.6	*V*
Supply current		300	*mA*
RF Input Voltage Swing (SE)		1.0	*V*
Case Temperature		+90	*ºC*
Storage Temperature	-40	+100	*ºC*
Operational Humidity	10	98	*%*
Storage Humidity	10	98	*%*

TERMINAL FUNCTIONS

TERMINAL			DESCRIPTION
Name	**No.**	**Type**	
High-Speed I/Os			
d0p	5	CML input	Differential data input signals with internal SE 50*Ohm* termination to vcc
d0n	3		
d1p	9	CML input	Differential data input signals with internal SE 50*Ohm* termination to vcc
d1n	11		
cp	23	CML input	Differential clock input signals with internal SE 50*Ohm* termination to vcc
cn	21		
qp	15	CML output	Differential data output signals with internal SE 50*Ohm* termination to vcc. Also require external SE 50*Ohm* termination to vcc
qn	17		
DC Control Inputs			
dcp	19	Analog inputs	Clock common mode control voltage
ampcrl	7		Output amplitude control voltage

Supply and Termination Voltages		
Name	**Description**	**Pin Number**
vcc	Positive power supply (+3.3*V* or 0)	2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24
vee	Negative power supply (0*V* or -3.3*V*)	1, 13

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ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vee	-3.1	-3.3	-3.5	*V*	±6%
vcc		0.0		*V*	External ground
*I*vee		245		*mA*	With maximum output amplitude
Power consumption		810		*mW*	
Junction temperature	-25	50	125	*°C*	
HS Input Data (d0p/d0n, d1p/d1n)					
Data rate	DC		64	*Gbps*	When used as a selector
Frequency	DC		56	*GHz*	When used as a selector
Data rate	DC		56	*Gbps*	When used as a multiplexer
Swing	100		800	*mV*	Differential or SE, p-p
CM Voltage Level	vcc-0.8		vcc	*V*	Must match for both inputs
HS Input Clock (cp/cn)					
Frequency	DC		56	*GHz*	
Swing	100		800	*mV*	Differential or SE, p-p
CM Voltage Level	vcc-0.8		vcc	*V*	Must match for both inputs
Duty cycle	45	50	55	*%*	
HS Output Data (qp/qn)					
Data rate	DC		64	*Gbps*	When used as a selector
Frequency	DC		56	*GHz*	When used as a selector
Data rate	DC		112	*Gbps*	When used as a multiplexer
Logic "1" level		vcc		*V*	
Logic "0" level	vcc-0.75		vcc-0.1	*V*	For ampcrl from vee to vcc and with external 50*Ohm* DC termination on each output
Rise/Fall times	3	4	5	*ps*	20%-80%
Output Jitter		1		*ps*	Peak-to-peak
Control Ports (dcp, ampcrl)					
Input Signal Range	vee		vcc	*V*	

DIE INFORMATION

The main dimensions of the die are given in Table 3.

Table 3. Important Die Dimensions

Pad metal dimensions	72μm x 72μm
Pad opening diameter	43μm
Die dimensions	1200μm x 1200μm

The part's die incorporates wire bonding pads with the coordinates of their centers given in Table 4.

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Table 4. Die Pad Coordinates

Pin Number	X Coordinate, *µm*	Y Coordinate, *µm*	Pin Number	X Coordinate, *µm*	Y Coordinate, *µm*
1	290	290	2	290	110
3	455	110	4	620	110
5	785	110	6	950	110
7	950	290	8	1130	290
9	1130	455	10	1130	620
11	1130	785	12	1130	950
13	950	950	14	950	1130
15	785	1130	16	620	1130
17	455	1130	18	290	1130
19	290	950	20	110	950
21	110	785	22	110	620
23	110	455	24	110	290

The part's identification label is ASNT5650-BD. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 2 characters after the dash represent the package's manufacturer, type, and pin out count.

This device complies with the Restriction of Hazardous Substances (RoHS) per 2011/65/EU for all ten substances.

REVISION HISTORY

Revision	Date	Changes
0.2.2	05-2020	Updated Die Information
0.1.2	08-2019	Updated Letterhead
0.1.1	08-2019	Corrected Terminal Functions table
0.0.1	08-2019	Preliminary release

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