Clock Divider Module  
PN L-6001-CD-2

DESCRIPTION

CD-2 is a clock divider module that plugs into the XBERT and ParalleX™ Chassis. With a divider input range of 100MHz – 20GHz, the module provides 4 selectable divide ratios of 1/2, 1/4, 1/8, 1/16 which can be changed via an easy to use GUI or front-panel push-button switch. Front panel indicators give immediate status of selected divide ratio. Although intended for use with the EBERT pattern generator/error detector, the CD-2 finds a variety of other applications as a clock divider.

KEY FEATURES

- 4 selectable divide ratios
  - 1/2
  - 1/4
  - 1/8
  - 1/16
- Divider input range 100MHz – 20GHz
- Differential clock input
- Differential clock output
- Clock input/outputs have single-ended capability (unused terminals should be terminated)
- Front panel switch for divide ratio selection
- LabView™ drivers available
- GPIB Interface via XBERT Chassis.
- Small size: width 25.4mm (1”)

XBERT PLATFORM: LETS YOU START SMALL AND GROW BIG

XBERT is a low-cost, modular Bit Error Rate Test Platform used for verification and test of 10Gb/s and above optical and electrical chip, sub assembly and system designs. ParalleX™ allows users to perform several BER tests at once using a single clock source. The system is ideal for developers desiring to run simultaneous BER tests on parallel interfaces or multiple independent interfaces. XBERT and ParalleX™ are scalable so users can start off with a single channel and add modules to grow the system. Manufacturers can realize great savings by taking advantage of the XBERT and ParalleX™ system’s scalability to perform parallel testing in volume production environments.
KEY PERFORMANCE PARAMETERS

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>Min</th>
<th>Max</th>
<th>UNIT</th>
<th>NOTE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clock Rate</td>
<td>CR</td>
<td>0.1</td>
<td>20</td>
<td>GHz</td>
<td>1</td>
</tr>
<tr>
<td>Clock Input Signal Channel</td>
<td>CLK INP/N</td>
<td>200</td>
<td>1000</td>
<td>mVpp</td>
<td>Note 2 Single ended</td>
</tr>
<tr>
<td>Clock Output Signal Channel</td>
<td>CLK OUTP/N</td>
<td>300</td>
<td>550</td>
<td>mVpp</td>
<td>Note 2 Single ended</td>
</tr>
<tr>
<td>Differential Input Impedance</td>
<td>Z_{in}</td>
<td>90</td>
<td>110</td>
<td>Ω</td>
<td></td>
</tr>
<tr>
<td>Differential Output Impedance</td>
<td>Z_{out}</td>
<td>90</td>
<td>110</td>
<td>Ω</td>
<td></td>
</tr>
<tr>
<td>Operating Temperature</td>
<td>T_{OP}</td>
<td>0</td>
<td>50</td>
<td>°C</td>
<td>Ambient temp.</td>
</tr>
</tbody>
</table>

Note:
1. 20GHz, if used at a divide ratio of 1/16.
2. If used single-ended, the other channel should be terminated in 50Ω to prevent output signal distortion.

GUI: allows selection of divide ratio