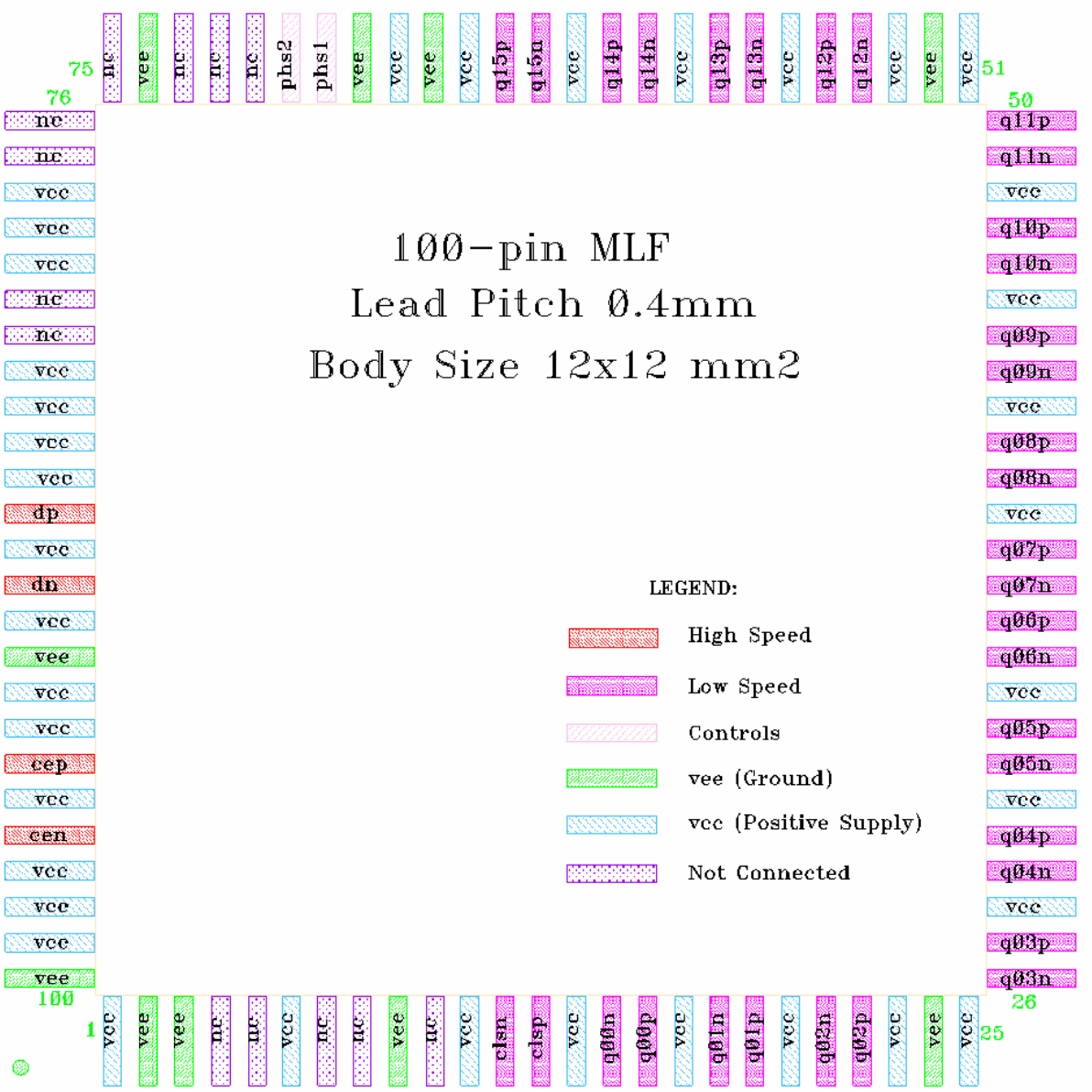
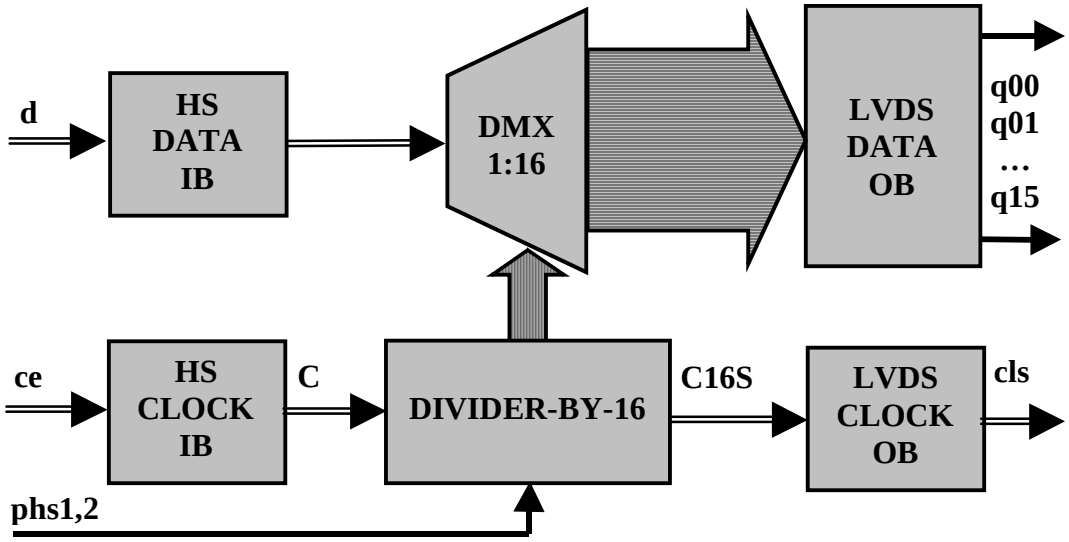
ASNT2011
12.5*Gbps* 1:16 Digital Deserializer

- Broadband up to 12.5*Gbps* (gigabits per second) 1:16 Deserializer
- High-speed Input Data Buffer with on-chip 100*Ohm* differential termination.
- Full-rate CML Input Clock Buffer with on-chip 50*ohm* single-ended (SE) termination to the positive supply rail ("vcc").
- LVDS Output Data Buffers with a proprietary low-power architecture.
- Clock-divided-by-16 LVDS Output Buffer with 90°-step phase selection
- Single +3.3*V* power supply.
- Industrial temperature range.
- Low power consumption of 600*mW* at 12.5*Gbps*.
- 100-pin MLF package.



27 Via Porto Grande, Rancho Palos Verdes, CA, 90275. Ph. # 1-310-377-6029. Fax # 1-310-377-9940.

DESCRIPTION



ASNT2011 is a digital broadband 1:16 deserializer supporting a serial input interface that can handle data rates up to 12.5*Gbps*. The primary application of ASNT2011 is to provide a high-speed input data channel for point-to-point data transmission over a controlled impedance media of 50*Ohm*. The transmission media can be a printed circuit board or copper coaxial cables. The functional distance of the data transfer is dependent upon the attenuation characteristics of the transportation media and the degree of noise coupling to the signaling environment.

During nominal operation, the serializer receives a high-speed differential serial data ("d") and a high frequency external differential clock ("ce") that is routed to an internal frequency divider (DIVIDER-BY-16). The divider generates internal clock signals with frequencies divided-by-2 (C2), divided-by-4 (C4), divided-by-8 (C8) and divided-by-16 (C16). An additional divided-by-16 clock signal with a 90º-step selectable phase delay (C16S) is also generated and controlled by CMOS signals "phs1,2".

A tree-type 1:16 demultiplexer (DMX1:16) latches the input serial data stream using both edges of the C2 clock generated by the divider. The data is subsequently deserialized and delivered to the outputs as low-speed 16-bit wide parallel words that are aligned to the C16 clock.

Proprietary low-power LVDS (Low voltage differential signaling) output buffers are used for the 16 low-speed data output channels (LVDS DATA OB) and the output low-speed clock (LVDS CLOCK OB). The buffers satisfy all the requirements of the IEEE Std. 1596.3-1996 and ANSI/TIA/EIA-644-1995.

ASNT2011 uses a +3.3*V* power supply and is characterized for operation at −25°C to 125°C of junction temperatures.

HS DATA IB

The High-Speed Data Input Buffer (HS DATA IB) accepts differential signals with a data rate up to12.5*Gbps*. The buffer utilizes an on-chip differential termination of 100*Ohm* for compatibility with the high-speed output buffer of the ASNT1011 serializer.

If CML input mode is required, the buffer can be used with additional external termination shown in the drawing below.

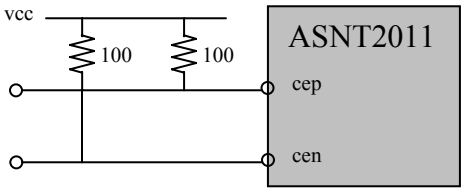


Fig. 1. External filter schematic

HS CLOCK IB

The High-Speed Clock Input Buffer (HS CLOCK IB) accepts differential signals with frequencies up to 12.5GHz. The buffer utilizes the standard on-chip CML single-ended termination of 50*Ohm* to the positive supply rail.

DIVIDER-BY-16

DIVIDER-BY-16 includes 4 divide-by-2 circuits connected in series. The high-speed input clock C is fed into the first divide-by-2 circuit that generates an output clock signal (C2) that is half the rate of the input clock. C2 is routed internally to the next divide-by-two circuit and outside of the block to MUX16:1. C4, C8, and C16 are formed and routed to MUX16:1 in a similar way.

In addition, C16 is passed onto the LVDS Clock Output Buffer (LVDS CLOCK OB) as the C16S signal. By utilizing the CMOS control pins “phs1” and “phs2”, the phase of C16S can be altered in accordance with the table below.

“phs1”	“phs2”	C16S phase
V_{EE} (default)	V_{EE} (default)	270°
V_{EE}	V_{CC}	180°
V_{CC}	V_{EE}	90°
V_{CC}	V_{CC}	0°

DMX1:16

DMX1:16 utilizes the standard half-rate tree architecture and latches the incoming high-speed data on both edges of the C2 clock signal that is supplied by DIVIDER-BY-16. The serial data stream is demultiplexed down and delivered to LVDS DATA OB in parallel fashion as16-bit wide words running at a data rate up to 781.25*Mbps*. The latency of this circuit block is equal to roughly one period of the low-speed input clock.

LVDS DATA OB

LVDS DATA OB accepts 16-bit wide words from DMX1:16 and converts them into LVDS output signals.

The proprietary low-power LVDS output buffer utilizes NPN HBTs that are common to standard BiCMOS technologies. It utilizes a special architecture that ensures operation at data rates up to 1*Gbps* with a low power consumption level of 20*mW*. The buffer satisfies all the requirements of the IEEE Std. 1596.3-1996 and ANSI/TIA/EIA-644-1995.

LVDS CLOCK OB

The LVDS Clock Output Buffer (LVDS CLOCK OB) receives the C16S signal from DIVIDER-BY-16 and converts it into an LVDS output signal. This is the same LVDS buffer as the one used for the data outputs.

TERMINAL FUNCTIONS

TERMINAL			DESCRIPTION
Name	No.	Type	
High-Speed I/Os			
cep	94	Input	CML differential high-speed clock inputs with internal SE 50*Ohm* termination to "vcc".
cen	96		
dp	87	Input	Differential high-speed data inputs with internal differential 100*Ohm* termination.
dn	89		
Controls			
phs1	69	LS In., CMOS	Low-speed output clock phase selection (default: both low).
phs2	70		
Supply and Termination Voltages			
vcc	many	PS	Positive power supply.
vee	many	PS	Negative power supply.
N/C	many		Unconnected pin.

TERMINAL			DESCRIPTION
Name	No.	Type	
Low-Speed I/Os			
q00n	15	Output	LVDS low-speed data outputs. Require external differential 100*Ohm* terminations.
q00p	16		
q01n	18		
q01p	19		
q02n	21		
q02p	22		
q03n	26		
q03p	27		
q04n	29		
q04p	30		
q05n	32		
q05p	33		
q06n	35		
q06p	36		
q07n	37		
q07p	38		
q08n	40		
q08p	41		
q09n	43		
q09p	44		
q10n	46		
q10p	47		
q11n	49		
q11p	50		
q12n	54		
q12p	55		
q13n	57		
q13p	58		
q14n	60		
q14p	61		
q15n	63		
q15p	64		
clsn	12	Output	LVDS low-speed clock outputs. Can transmit four different clock phases as defined by “phs1” and “phs2”..
clsp	13		

27 Via Porto Grande, Rancho Palos Verdes, CA, 90275. Ph. # 1-310-377-6029. Fax # 1-310-377-9940.

ELECTRICAL CHARCTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
V_{CC}	3.14	3.3	3.47	*V*	±5%
V_{EE}		0.0		*V*	
V_{ECL}		V_{CC}-2.0		*V*	
Power consumption		600		*mW*	
Junction temperature	-25	50	125	*°C*	
HS Input Data (d)					
Data Rate	8.0		12.5	*Gbps*	
Standard voltage swing	0.3			*V*	Single-ended
Common mode voltage	V_{CC}-0.7		V_{CC}-0.2	*V*	DC
HS External Clock (ce)					
Frequency		8 or 12.5		*GHz*	
Logic “1” level		V_{CC}		*V*	
Logic “0” level			V_{CC}-0.25	*V*	
Duty Cycle	40%	50%	60%		
LS Output Data (q0-q15)					
Data Rate	500		800	*Mbps*	
Interface		LVDS			Meets the IEEE Std. 1596.3-1996
LS Output Clock (cls)					
Frequency	500		800	*MHz*	
Interface		LVDS			Meets the IEEE Std. 1596.3-1996
CMOS Control Inputs					
Logic “1” level	V_{CC}-0.4			*V*	
Logic “0” level			V_{EE}+0.4	*V*	
Timing Parameters					
“cls” to “q0-q15” delay variation		±2.5%			Over the full temperature range