**General Description**

The iT4036F is an ultra-wideband phase delay designed with a high-speed ECL topology for either single-ended or differential data input/output. Its high speed (up to 12.5 Gb/s), excellent rise and fall times, and eye diagram quality make the iT4036F suitable for timing adjustment in data and clock distribution. Demanding digital applications benefit from the iT4036F, including clock data recovery, edge detectors, NRZ-to-RZ converters, MUX/DEMUX, data restoration, PSK modulation schemes.

The device features a single delay element that provides up to 120-ps delay. Delay control can be either differential (using both Vcp and Vcn) or single-ended (Vcn is the active control pad while Vcp is shorted to Vcref). The control voltage range for the delay input is from -1.3 V to -1.9 V regardless of whether the control is single-ended or differential. The device can delay NRZ streams at data rates up to 12.5 Gb/s or clock signals up to 11.7 GHz. Both inputs and outputs are DC-coupled and feature internal 50-ohm resistors at the inputs and outputs. The iT4036F is housed in a 5x5-mm RoHS-6-compliant QFN package.

**Applications**

- OC-192/STM-64 Transmission Systems
- 10Gbps Systems using Optical Amplifiers
- High speed clock data recovery
- Wideband phase modulation
- Jitter Injection

**Features**

- Ultra wideband: Up to 12.5 Gb/s NRZ or 11.7 GHz Clock Signals
- Delay adjustment up to 120 ps
- 400 mVpp single-ended output
- Low RMS jitter degradation
- Output rise time (20%/80%): 24 ps
- Output fall time (20%/80%): 22 ps
- 50-ohm matched AC or DC-coupled I/O
- Differential or single-ended I/O
- Power consumption: 570 mW
- Cascadable to obtain n*120 ps of delay without requiring buffers between devices.
- 5x5-mm RoHS-6-compliant QFN

**Device Diagram**

![Device Diagram](image-url)
Absolute Maximum Ratings

Exceeding the maximum ratings may cause damage to this product or lead to a reduction in reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature. AC and DC device characteristics at or beyond the absolute maximum ratings are not assured or implied.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{EE}</td>
<td>Power supply voltage</td>
<td>-4.0</td>
<td>0</td>
<td>V</td>
</tr>
<tr>
<td>V_{IN}</td>
<td>Input voltage level at each RF port</td>
<td>-0.9</td>
<td>0.5</td>
<td>V</td>
</tr>
<tr>
<td>V_{cp}, V_{cn}</td>
<td>Delay control voltage</td>
<td>-2.2</td>
<td>-1.1</td>
<td>V</td>
</tr>
<tr>
<td>I_{cp}, I_{cn}</td>
<td>Delay control current</td>
<td>0</td>
<td>2</td>
<td>mA</td>
</tr>
<tr>
<td>T_{B}</td>
<td>Operating temperature range – package base</td>
<td>-15</td>
<td>125</td>
<td>°C</td>
</tr>
<tr>
<td>T_{STG}</td>
<td>Storage temperature</td>
<td>-65</td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>

Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{EE}</td>
<td>Power supply voltage</td>
<td>-3.46</td>
<td>-3.30</td>
<td>-3.13</td>
<td>V</td>
</tr>
<tr>
<td>V_{cp}, V_{cn}</td>
<td>Delay controls voltage (1)</td>
<td>-1.9</td>
<td>-1.3</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>V_{INDC}</td>
<td>DC input voltage (2,3)</td>
<td>-0.4</td>
<td>-0.2</td>
<td>0</td>
<td>V</td>
</tr>
<tr>
<td>V_{IN}</td>
<td>S.E. Data input voltage amplitude (3)</td>
<td>0.2</td>
<td>0.4</td>
<td>0.6</td>
<td>Vpp</td>
</tr>
<tr>
<td>T_{B}</td>
<td>Operating temperature range – package base (4)</td>
<td>0</td>
<td>85</td>
<td>°C</td>
<td></td>
</tr>
</tbody>
</table>

Note

1. See “Recommended delay controls configuration” for further details
2. Valid for DC coupling only
3. With a single-ended input, the unused pad must be tied to V_{INDC} (DC coupling) or to ground (AC coupling)
4. May require heat sink. Exceeding maximum temperature will lead to a reduction in reliability
Wideband Phase Delay

**Electrical Characteristics**

Measured at $T_{BASE}=25^\circ C$, $V_{EE} = -3.3V$

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{cref}$</td>
<td>Internal Voltage Reference (1)</td>
<td>-1.65</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{OUTDC}$</td>
<td>DC output voltage (2,3)</td>
<td>-0.25</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{OUT-NRZ}$</td>
<td>S.E. Data output voltage amplitude 12.5Gb/s(3)</td>
<td>0.40</td>
<td></td>
<td></td>
<td>Vpp</td>
</tr>
<tr>
<td>$V_{OUT-Clock}$</td>
<td>S.E. Clock output voltage amplitude at 11.7GHz(3)</td>
<td>0.35</td>
<td></td>
<td></td>
<td>Vpp</td>
</tr>
<tr>
<td>$T_R$</td>
<td>Output rise time (20% – 80%)</td>
<td>24</td>
<td></td>
<td></td>
<td>ps</td>
</tr>
<tr>
<td>$T_F$</td>
<td>Output fall time (20% – 80%)</td>
<td>22</td>
<td></td>
<td></td>
<td>ps</td>
</tr>
<tr>
<td>$Jit_{Deg}$</td>
<td>RMS Jitter deg – PRBS $2^{31}$ NRZ data at 12.5Gb/s (4)</td>
<td>3</td>
<td></td>
<td></td>
<td>ps</td>
</tr>
<tr>
<td>$T_{ADJ}$</td>
<td>Maximum phase delay adjustment</td>
<td>110</td>
<td>120</td>
<td></td>
<td>ps</td>
</tr>
<tr>
<td>$T_{DH} T_{DL}$</td>
<td>Insertion delay (5)</td>
<td>200</td>
<td></td>
<td></td>
<td>ps</td>
</tr>
<tr>
<td>$S_{11}$</td>
<td>Input return loss (up to 15 GHz)</td>
<td>10</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>$S_{22}$</td>
<td>Output return loss (up to 15 GHz)</td>
<td>10</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>$F_{data\ max}$</td>
<td>Maximum NRZ data rate (6)</td>
<td>12.5</td>
<td></td>
<td></td>
<td>Gb/s</td>
</tr>
<tr>
<td>$F_{clock\ max}$</td>
<td>Maximum clock frequency (6)</td>
<td>11.7</td>
<td></td>
<td></td>
<td>GHz</td>
</tr>
<tr>
<td>$I_{EE}$</td>
<td>Power supply current</td>
<td>175</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>$P_D$</td>
<td>Power dissipation</td>
<td>0.57</td>
<td></td>
<td></td>
<td>W</td>
</tr>
</tbody>
</table>

**Notes**

1. To use the delay control single ended tie the unused one to $V_{cref}$ or to an external high precision voltage reference
2. Valid for DC coupling only
3. With a single-ended output, the unused pad must be terminated with 50 ohm to ground
4. $J_{rms} = \sqrt{\frac{1}{T_{ADJ}} \int_{t=0}^{T_{ADJ}} (J(t))^2 \, dt}$
5. Insertion delay with $V_{cp}/V_{cp}$ set for the minimum output delay. For example, for a device with $T_{DH} = T_{DL} = 200$ps and $T_{ADJ} = 120$ps, the total insertion delay can vary from a minimum of 200ps to a maximum of 200+120=320ps adjusting the $V_{cp}/V_{cp}$ (See Figure 2)
6. Please note, measured at 25°C
Electrical Performance

Figure 2 Timing Diagram

Figure 3 Jitter degradation vs Vcn (with Vcp tied to Vref)
Wideband Phase Delay

Eye Diagram Performance

- Evaluation board measurement at
  - $V_{ee} = -3.3V$, Temperature = 25°C
  - Single-ended input: 450mVpp
  - $J_{rms} = \sqrt{J_{meas}^2 - J_{thru}^2}$

![Figure 4 Through eye at 12.5Gb/s](image-url)
Eye Diagram Performance (cont)

Figure 5  Input data rate: 12.5 Gb/s
Control voltage: $V_{cp} = V_{cref}, V_{cn} = -1.6$ V
Jitter degradation: 1.1ps RMS
(Delay 50ps, 225 deg.)

Figure 6  Input data rate: 12.5 Gb/s
Control voltage: $V_{cp} = V_{cref}, V_{cn} = -1.9$ V
Jitter degradation: 0.6ps RMS (Delay 120 ps, 540 deg.)
Wideband Phase Delay

Eye Diagram Performance (cont)

Figure 7 Input data rate: 10.7 Gb/s
Control voltage: \( V_{CP} = V_{cref}, V_{CN} = -1.6V \)
Jitter degradation: 0.5ps RMS
(Delay 50ps)

Figure 8 Input data rate: 10.7 Gb/s
Control voltage: \( V_{CP} = V_{cref}, V_{CN} = -1.9V \)
Jitter degradation: 0.2ps RMS
(Delay 120ps)
Figure 9 Clock signal at 12.5GHz
Single-ended data input: +/-200 mVpp

Figure 10 Clock signal at 11.5GHz
Single-ended data input: +/-200 mVpp
Eye Diagram Performance (cont)

Figure 11 Clock signal at 12.5GHz
Single-ended data input: +/-200mVpp
Vcm span from –1.3V to –1.9V

Temperature Characterization

Figure 12 Iee vs Temperature
Temperature Characterization (cont)

Figure 13 Output Voltage vs Temperature

Figure 14 Delay drift over Temperature with Vcp tied to Vref.
Recommended Operational Setup

Figure 15 Recommended operating setup

Notes

1. Each Vee pin requires two decoupling capacitors. The recommended values are 560pF and 0.1uF.
2. The decoupling network attached to pin 8 (V_{cp}) and 9 (V_{cref}) is only required for single ended delay control operation.
3. For best performance, physical place the smaller capacitor (560pF) closer to the device pin than the larger capacitor (0.1uF).
**Biasing Procedure**

To power up the device:

1. Connect the $V_{cp}$ to
   a. $V_{ref}$ (for S.E. delay control) OR
   b. an external high precision voltage reference (for S.E. delay control) OR
   c. an external variable voltage source and set a value between -1.3V and -1.9V

2. Connect the $V_{cn}$ to
   a. $V_{ref}$ (for S.E. delay control) OR
   b. an external high precision voltage reference (for S.E. delay control) OR
   c. an external variable voltage source and set a value between -1.3V and -1.9V

3. Set the $V_{EE}$ at -3.3V

4. Adjust $V_{cn}/V_{cp}$ to tune the output delay (see “Recommended delay control configurations” for further details)
   - Never exceed the absolute maximum ratings for $V_{cn}/V_{cp}$ and $I_{cn}/I_{cp}$.
   - These currents must always be less than 2mA, see fig. 16 Safe Operating Area.
   - Do not to power up the device ($V_{ee} = -3.3V$) with $V_{cn}/V_{cp}$ still at ground.

To power down the device:

1. Set the $V_{EE}$ to GND

2. Set $V_{cn}$ and $V_{cp}$ to ground

---

**Figure 16 Safe Operating Area**
Recommended I/O Configurations

Figure 17 I/O Configurations. Any depicted I/O combination is allowed (for example the input can be differential DC coupled and the output single ended AC coupled or vice versa)
Recommended Delay Control Configurations

**Differential Delay Control**

![Differential Delay Control Diagram]

**SE Vcn Delay Control**

![SE Vcn Delay Control Diagram]

**SE Vcp Delay Control**

![SE Vcp Delay Control Diagram]

Figure 18 Delay Configurations
Wideband Phase Delay

Input buffer diagram

Output buffer diagram

Figure 19 iT4036F Input Output buffers
**Notes**

- Signal path delay is controlled using the Vcn and Vcp in either differential or single ended configurations.
- The differential configuration provides more bandwidth and noise immunity and is recommended for sensitive applications such as jitter injection and phase modulation.
- The single ended configuration is recommended for low bandwidth applications such as CDR (clock data recovery) and skew compensation.
- Vcref is provided to simplify single ended configurations
  - Vcref can be tied to Vcp and thus Vcn is used to adjust the delay through the device.
  - Vcref can be tied to Vcn and thus Vcp is used to adjust the delay through the device.
  - The decision on which pin to use should be based upon the direction of the feedback loop desired, please see delay configurations on page 14 for further information.
Wideband Phase Delay

Form Description

Package

Figure 21 iT4036F Package Dimensions

<table>
<thead>
<tr>
<th>Pad</th>
<th>Name</th>
<th>Pad</th>
<th>Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Vee</td>
<td>11</td>
<td>Vee</td>
</tr>
<tr>
<td>2</td>
<td>Din</td>
<td>12</td>
<td>Dout</td>
</tr>
<tr>
<td>3</td>
<td>Not connected</td>
<td>13</td>
<td>Not connected</td>
</tr>
<tr>
<td>4</td>
<td>Din/</td>
<td>14</td>
<td>Dout/</td>
</tr>
<tr>
<td>5</td>
<td>Vee</td>
<td>15</td>
<td>Vee</td>
</tr>
<tr>
<td>6</td>
<td>Not connected</td>
<td>16</td>
<td>Not connected</td>
</tr>
<tr>
<td>7</td>
<td>Vcn</td>
<td>17</td>
<td>Not connected</td>
</tr>
<tr>
<td>8</td>
<td>Vcp</td>
<td>18</td>
<td>Not connected</td>
</tr>
<tr>
<td>9</td>
<td>Vcref</td>
<td>19</td>
<td>Not connected</td>
</tr>
<tr>
<td>10</td>
<td>Vee</td>
<td>20</td>
<td>Not connected</td>
</tr>
</tbody>
</table>
iT4036 Wideband Phase Delay

Ordering Information

<table>
<thead>
<tr>
<th>Part</th>
<th>Temp Range</th>
<th>Pin-Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>iT4036F</td>
<td>0°C to +85°C</td>
<td>5x5mm QFN RoHS-6 Compliant</td>
</tr>
<tr>
<td>iT4036FEVB</td>
<td>N/A</td>
<td>Evaluation Board</td>
</tr>
</tbody>
</table>

Application Information

CAUTION: HIGH POWER DEVICE

- Do not exceed junction temperature of 150°C. A heat sink and low impedance thermal path is required.
- RF Microwave devices are capable of high energy densities at the RF output; user application may be required to meet SAR (Specific Absorption Rate) regulatory safeguards.
- This is an extremely fast high bandwidth digital device capable of high level harmonic emissions that are normal components of a high fidelity pulse. Care may be required to meet regulatory intentional or unintentional system emission requirements.

CAUTION: ESD-SENSITIVE DEVICE

- Less than 250V HBM ESD discharge may damage the device.
- Class 0 Device, JES22-A114E